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COPYBIT ELIMINATOR REVISITED

Design by H. Schaake

Our February 1994 issue carried an article describing an inexpensive and straightforward circuit for eliminating the copybit from a digital S/PDIF* audio signal to enable users to copy (digitally) their own musical work many times without degradation by the SCMS**. The present article describes an updated version of that circuit, which can be used with the latest DAT, DCC and MD players.

A comparison

The integrated circuits used in digital recorders fulfil more and more functions. Even the until recently discrete S/PDIF buffer/amplifier which converts the S/PDIF signal to TTL level is integrated in modern equipment. This is a good thing, of course, since fewer ICs bring the cost, and thus the price to the consumer, down.

The original eliminator needed a TTL signal at its input, but the updated version contains a separate S/PDIF buffer amplifier. However, the design allows S/PDIF signals already at TTL level to be processed without any difficulty.

The ICs used in modern recorders are faster and run at a higher master-clock frequency than those produced only a few years ago. Nowadays, a $256f_s$ master clock is quite normal, and even $384f_s$ and $512f_s$ models are in production. Since the eliminator needs a $128f_s$ clock, a binary scaler is provided in the updated version. If a $128f_s$ clock is available in the recorder and this can be used, it should be preferred: experience shows that this enables some recorders to lock on more readily.

The present version provides a choice of using either a LOCK or an UNLOCK signal and the facility of inverting the clock if required. These options may be useful for modifying types of DAT, DCC or MD recorder that have not been considered by the designer.

The copybit indication outputs, COPYIN and COPYOU, can not only drive LEDs directly, but may be used, if a copybit is present, as a block (=192 frames) trigger. This allows the S/PDIF signal to be inspected on an oscilloscope at or near the timing-slot position of the copybit frame.

The circuit

The circuit of the original version has been complemented with an IC (by using a MACH210 in the IC_1 position), a couple of resistors, some jumpers, and a capacitor—see Fig. 1. The MACH210 is equivalent to two MACH110s (used in the earlier version), These chips are identical as far as housing is concerned.

The operation of the updated eliminator is identical to that of the earlier version: the reader is therefore referred to the earlier article for background information, block schematic and timing diagram.

Construction

The printed-circuit board in Fig. 3 has been kept small to facilitate its incorporation into a recorder.

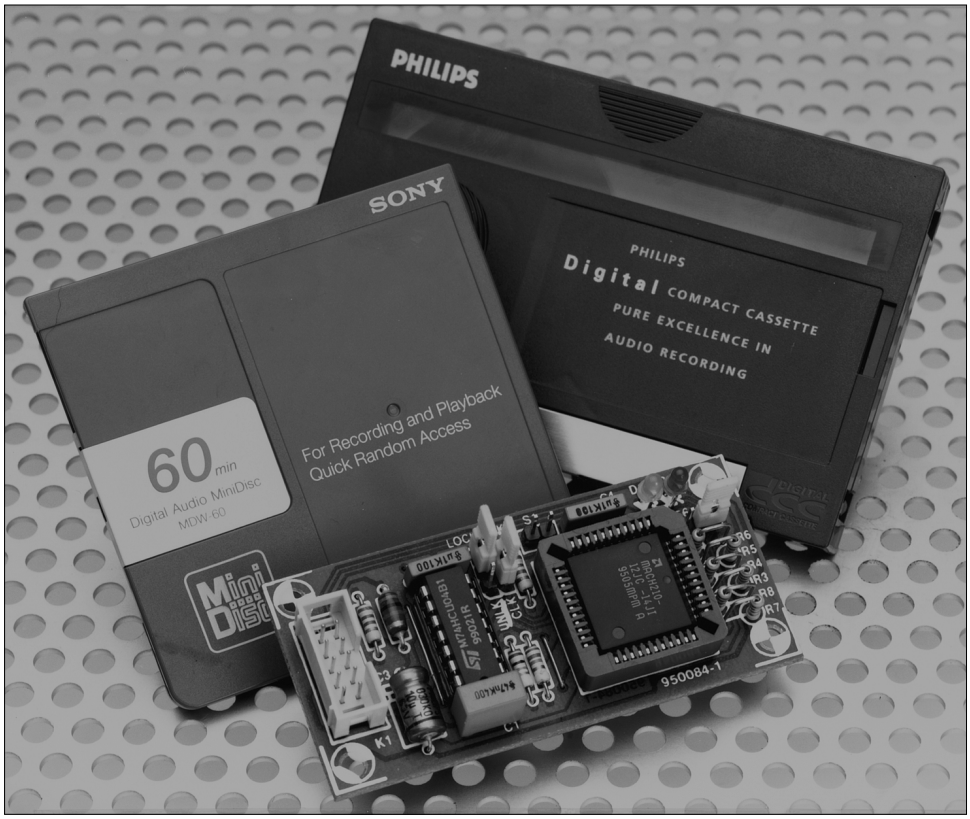
Population of the board is straightforward. The MACH210 is housed in a PLCC case. One of the four corners has been chamfered to indicate how the chip should be located in the relevant IC socket.

Header K_1 is signal-compatible with the earlier version.

A length of flatcable (keep this as short as possible) terminated into a 10-pin connector links the circuit with the appropriate points in the recorder. Switch S_1 enables the eliminator to be switched on and off as required. Thus, if the eliminator is intended to be in circuit at all times, the switch may be omitted.

Building into a recorder

Selecting between CLK and CLK, UNLK and LOCK, and $128f_s$ and $256f_s$ is by means of jumpers. The table on the next page gives connection data for a number of modern recorders; these data may also prove useful with recorders not specified. The selection between CLK and CLK is not given; this must be determined empirically, since



* Sony/Philips Digital Interface Format – the consumer version of the AES/EBU standard. This standard was devised by the American Audio Engineering Society and the European Broadcasting Union to define the signal format, electrical characteristics and connectors to be used for digital interfaces between professional audio products.
** Serial Copy Management System.

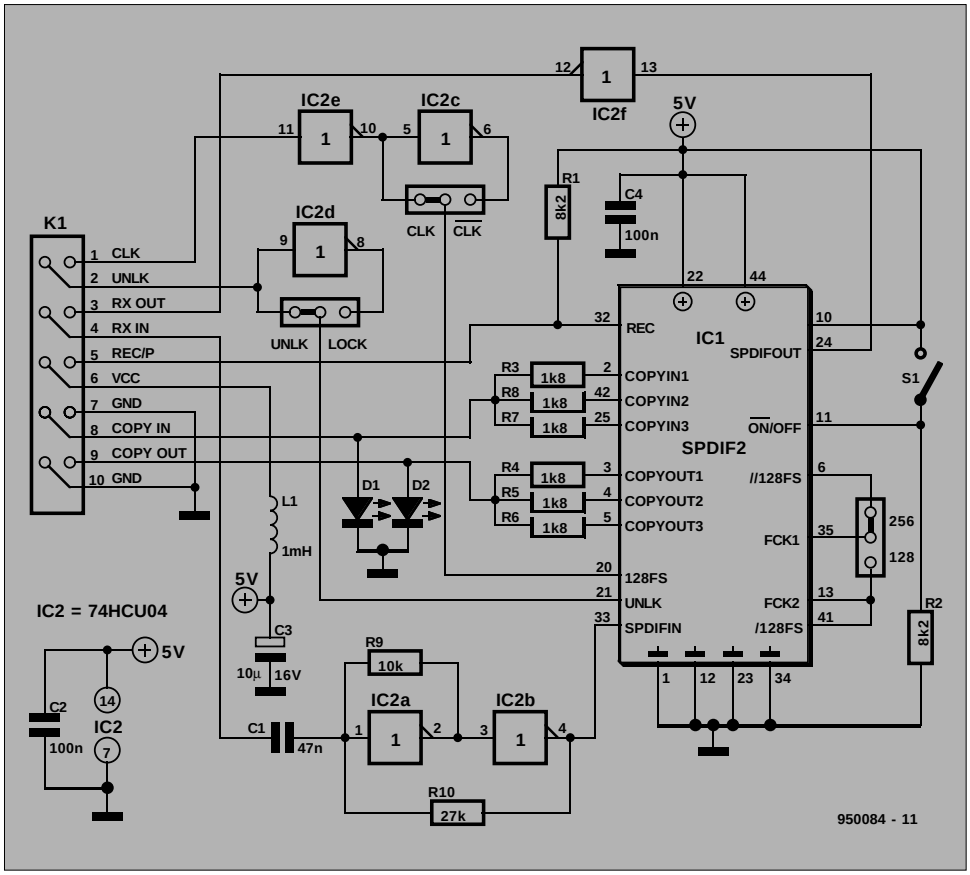


Fig. 1. Circuit diagram of the updated copybit eliminator.

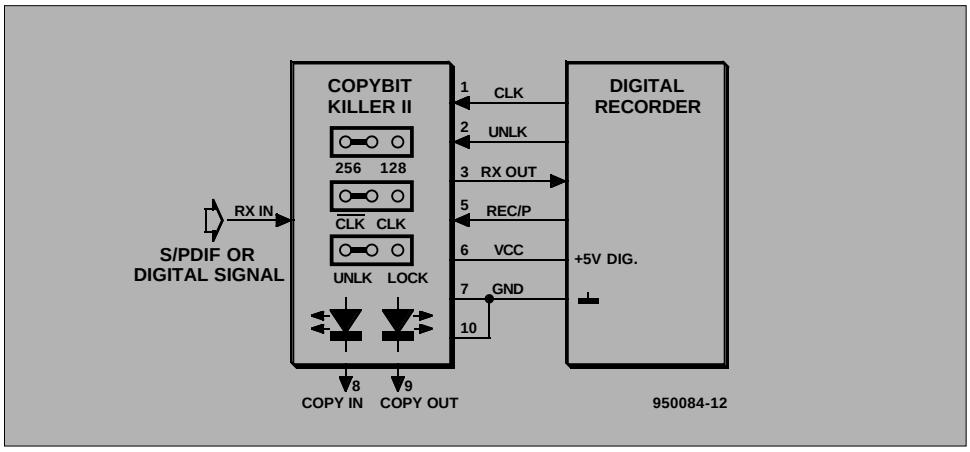


Fig. 2. Interconnection diagram of the signal source, the updated copybit eliminator and the recorder.

it depends on other connections. This involves nothing more than reversing the jumper and seeing whether the recorder locks or does not lock to the digital audio data of the eliminator.

If the connections of a particular recorder are not given, order a service manual in which these can normally be found.

A typical interconnection diagram of the signal source, the updated copybit eliminator and a digital recorder is given in Fig. 2.

Pin signals

Pin 1 (CLK). This is either $128f_s$ or $256f_s$, depending on the position of jumper 128/256. A jumper at CLK gives an inverted clock signal; at CLK, it gives a direct clock signal.

Pin 2 (UNLK). This gives the PLL lock indication. The signal must be low when the PLL is locked (jumper at UNLK). If the opposite is the case, set the jumper in position LOCK.

Pin 3 (RXOUT). The relevant track on the board is broken before or after the coaxial/optical S/PDIF input buffer, depending on the accessibility of these points in the recorder. The part of the track from the input bus or the output of the buffer is linked to RXIN and the other part to RXOUT.

Pin 4 (RXIN). See text for pin 3.

Pin 5 (REC/P). The record indication signal is connected to this pin (high level when the equipment is recording).

Pin 6. (VCC). Supply voltage (+5 V) tapped from the recorder.

Pin 7 (GND). Link to ground of recorder.

Pins 8, 9, 10 are for connecting remotely sited LEDs. The signals may also be used as block trigger for inspecting the S/PDIF signal on an oscilloscope (only possible when the copybit is present in the input signal).

Parts list

Resistors:

R_1, R_2 = 8.2 kΩ
R_3–R_8 = 1.8 kΩ
R_5 = 27 kΩ
R_9 = 10 kΩ

Capacitors:

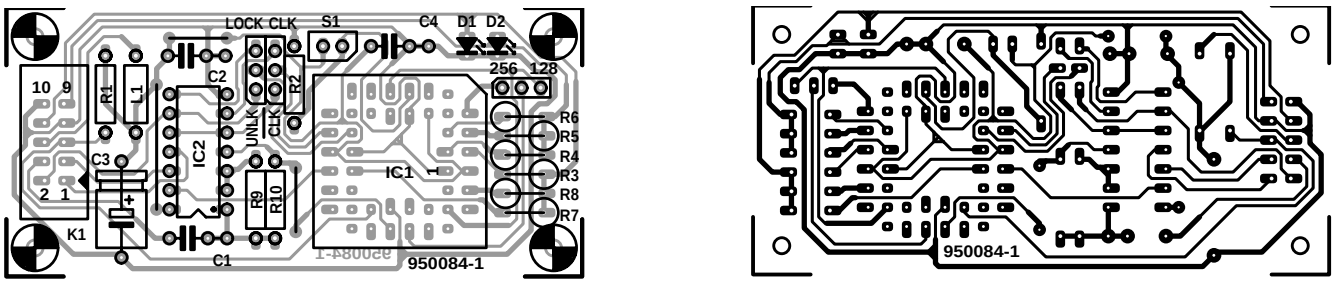


Fig. 3. Printed-circuit board for the updated copybit eliminator.

Contents

C_1 = 47 nF
C_2, C_4 = 100 nF
C_3 = 10 µF, 16 V

Semiconductors:
D_1 = LED, 3 mm, yellow
D_2 = LED, 3 mm, red

Integrated circuits:
IC_1 = MACH210 (Order no. 956504-1† – see p. 70)
IC_2 = 74HCU04

Inductors:
L_1 = 1 mH

Miscellaneous:
K_1 = 10-way right-angle box header
S_1 = switch with single make contact
PCB Order no. 950084† (see p. 70)

† The board and IC_1 may be ordered as a package: Order no.950084-C

[950084]

K_1 pin no.	Connect in recorder to	Remarks	Jumpers on PCB
Sony MDS-101 (MD recorder)			
1 (CLK)	IC_{510} pin 21 (128f_s)		128
	or IC_{505} pin 6 (256f_s)		256
2 (UNLK)	IC_{103} pin 5		LOCK
3 (RXOUT)	IC_{103} pin 65		
4 (RXIN)	CNP_{103} (connector) pin 4	break track between through metallization and connector	
5 (REC/P)	IC_{111} pin 70		
6 (VCC)	CNP_{103} pin 7		
7 (GND)	CNP_{103} pin 6		
Philips DCC-900 (DCC recorder)			
1 (CLK)	Q_{441} pin 26 (256f_s)		256
2 (UNLK)	Q_{441} pin 9		UNLK
3 (RXOUT)	coaxial: J_{421} (connector) pin 7	at mother board side	
	optical: J_{421} (connector) pin 3	at mother board side	
4 (RXIN)	signal side of C_{457} (150 pF)	break track to J_{421}	
5 (REC/P)	not known	link to VCC	
6 (VCC)	J_{421} (connector) pin 25		
7 (GND)	J_{421} (connector) pin 4		
Sony DTC-59ES (DAT recorder)			
1 (CLK)	IC_{307} pin 58 (128f_s)		128
2 (UNLK)	IC_{307} pin 31		UNLK
3 (RXOUT)	IC_{302} pin 6		
4 (RXIN)	IC_{301} pin 8	break track to this pin	
5 (REC/P)	IC_{309} pin 9		
6 (VCC)	IC_{322} pin 3	fit heat sink on to IC	
7 (GND)	chassis		
Sony DTC-690 (DAT recorder)			
1 (CLK)	R_{320} (256f_s)		256
2 (UNLK)	eponymous wire bridge		UNLK
3 (RXOUT)	IC_{302} pin 6		
4 (RXIN)	R_{316} at side of IC_{302}	disconnect resistor at IC_{302} side	
5 (REC/P)	not known	link to VCC	
6 (VCC)	eponymous wire bridge		
7 (GND)	eponymous wire bridge		
Sony DTC-750ES (DAT recorder)			
1 (CLK)	IC_{307} pin 58 (128f_s)		128
2 (UNLK)	IC_{307} pin 31		UNLK
3 (RXOUT)	IC_{307} pin 52		
4 (RXIN)	IC_{301} pin 8	break track to this pin	
5 (REC/P)	IC_{309} pin 8		
6 (VCC)	IC_{322} pin 3	fit heat sink on to IC	
7 (GND)	chassis		

Connections between K_1 and relevant points in various recorders.