Contents

COPYBIT INVERTER

WARNING. The information in this article is intended solely for the recording, processing and copying of private musical work. The Editor and Publishers disclaim all responsibility for any use that may infringe any copyright vested in commercial compact discs and (digital) tape cassettes.

The copybit eliminator published in the February 1994 issue of this magazine has two drawbacks. The first of these is that it cannot be used without modifying the digital audio equipment. The second is clear from the revisit to the eliminator in the September 1995 issue: from time to time, the eliminator needs updating – it is not 'future-proof'. The copy-permit converter described in this article does not have these drawbacks

Design by W. Foede

Like the copybit eliminator published in this magazine in the February 1994 and September 1995 issues, the copybit inverter is an inexpensive and simple-to-build circuit for inverting the copybit in a digital S/PDIF* audio signal to enable users to copy (digitally) their own musical work many times without degradation by the SCMS**.

The inverter can be included in the S/PDIF link between any digital a.f. signal source (such as a DCC recorder, a CD player, a DSR receiver) and a (second) DCC recorder without the need of opening or modifying any of the equipment. During the copying, any copybit is inverted and at the same time the category code is altered. This means that the S/PDIF signal so modified is accepted by the recorder as if it comes from a CD player (so that unlimited copying of the signal becomes possible). The inverter also offers a number of other facilities, such as S/PDIF detection.

Category code

The coding of the S/PDIF has been described in detail in the article on the 'Copybit eliminator'. The following description is therefore limited to the most important aspects of it.

In all domestic audio equipment, the format uses sample frequencies of 32 kHz, 44.1 kHz and 48 kHz. These data contain, among others, information as to the copybit. The format reacts to the content of the S/PDIF. The SCMS, which inhibits multiple (digital) copying of the source signal, can be bypassed as shown in the flow diagram in Fig. 1. It is not sufficient to invert only copybit 1. As the diagram shows, when copying with category code 00 000 000 (general) takes place, for instance, the copybit is not sampled. This means that the recording has to be passed through a copybit eliminator a second time. It is, therefore, much safer to set the copybit to (or hold it at) 1 and assign to it the category code of an apparatus whose copybit is always sampled.

The present inverter always outputs the category code of a DAT or a CD, depending on the input signal. The code changes automatically, so that the subdata in the USER channel of the relevant equipment are retained.

The unit can be used as a converter with either optical or coaxial inputs and outputs without any change in the input signal.

The left-hand and right-hand channels

Brief specification

- Opening or modification of the audio equipment not required
- 'Future-proof', since it is independent of the category code
- Unlimited (digital) copying of source material
- Optical or coaxial inputs and outputs as required
- S/PDIF detector
- Indication of the position of the copybit and automatic setting to 1 (= digital copying permitted)
- Indication of the category code and automatic setting to 10 000 000 (CD) or 11 000 000 (DAT)
- AES/EBU format can be copied
- Transparent USER-Subcode channel
- Indication as to whether operation is as converter or as inverter
- Minimal number of components
- Non-critical setting up without test instruments

* Sony/Philips Digital Interface Format – the consumer version of the AES/EBU standard. This standard was devised by the American Audio Engineering Society and the European Broadcasting Union to define the signal format, electrical characteristics and connectors to be used for digital interfaces between professional audio products.
** Serial Copy Management System.

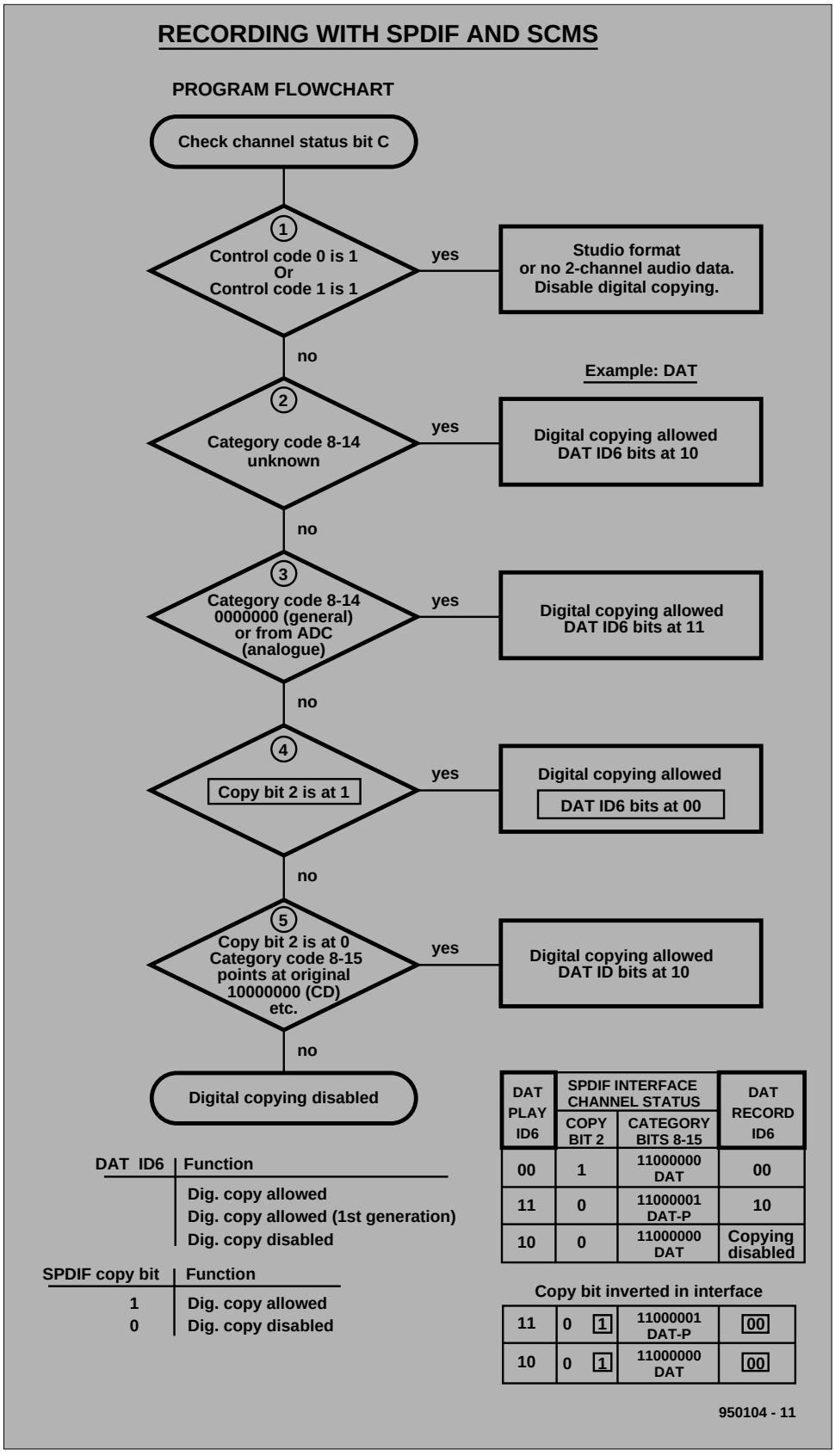


Fig. 1. Flow diagram of the evaluation process of the copybit in an S/PDIF signal.

each build a subframe of 32 bits, which together form a frame of 64 bits with a sampling frequency of, say, 44.1 kHz. A block contains a total of 192 frames (or 384 subframes) as shown in Fig. 2. The data are transmitted in biphase mark code, in which a bit is split into two bit-cells. In case of a digital 0, both cells have the same level, that is, 00 or 11. In case of a logic 1, the levels of the cells are inequal, that is, 01 or 10, which means that there is a level change at the centre of the bit. The longest a level can last is thus 1 bit—see Fig. 3.

This process also means that the clock is included in the transmitted information.

So as to identify the subframes and the start of the block, eight bit-cells have a bit sequence that does not occur in the biphase code—see Fig. 4. They are the block preamble *B*, which also identifies the left-hand channel in subframe 0, subframe preamble *M* (left-hand channel) and subframe preamble *W* (right-hand channel).

For the inversion of the SCMS, only bit 30, the channel status bit *C* of each subframe, is of importance. A complete channel status is repeated in each block of 384 subframes. The assignment of copy and category is the same in both channels.

The copybit is contained in subframes 4 and 5, and the category code in subframes 16–31.

Bits 30 and 31 in frame 15 have a special meaning. The so-called generation bit indicates whether the signal is an original or a copy. The assignment of a level for the original signal depends o the equipment. When the copybit is 0, bits C_{15} are sampled. An original signal permits one copy, and this must be an analogue copy. When the copybit is 1, no sampling takes place. To avoid any interference in the biphase code, two successive bits must be altered in the left-hand and right-hand channels respectively.

Reverting to the data contained in the user bit. only parity bit *P* needs to be considered as adjacent second bit. This thus determines the parity.

Conversion with PLD chip

The block diagram of the copybit inverter is shown in Fig. 7, and the circuit diagram in Fig. 8.

The digital a.f. signal – 0.5 V_{pp} into 75 Ω – is coupled capacitively to inverter IC_{1a}, which is arranged as an amplifier. The standard circuit is an inverter with feedback, but this has the disadvantage that the circuit tends to oscillate with open input. In the present circuit, the operating point is set permanently with P_1.

Inverter IC_{1a} is followed by a delay circuit with a delay time of 120 ns.

To ensure that both inputs (optical and coaxial) provide equal signal levels, the output of the opto-receiver, which is about 1.5 V_{pp}, is applied to the coaxial input via R_8. A change-over switch is not needed, since R_8 decouples both inputs adequately. In optical operation, the signal can thus be taken straight from the coaxial socket.

The direct and delayed signals are XOR-gated in IC_2 This makes the signal independent of the polarity at the input, since all subsequent steps are related to the XOR signal. The spacing of the positive edge in case of a logic 0 is 354 ns and in case of a logic 1, 177 ns—see Fig. 5.

Normally, the clock is retrieved by a phase-locked loop, PLL, which, as far as time and phase ratios are concerned, is not easily kept stable. Moreover, the voltage-controlled oscillator, VCO, remains operational in the absence of an input signal, which makes decoding of the block and subframe clocks more complicated.

The XOR signal starts non-retriggerable monostable IC_{3a}, which has a dwell time of

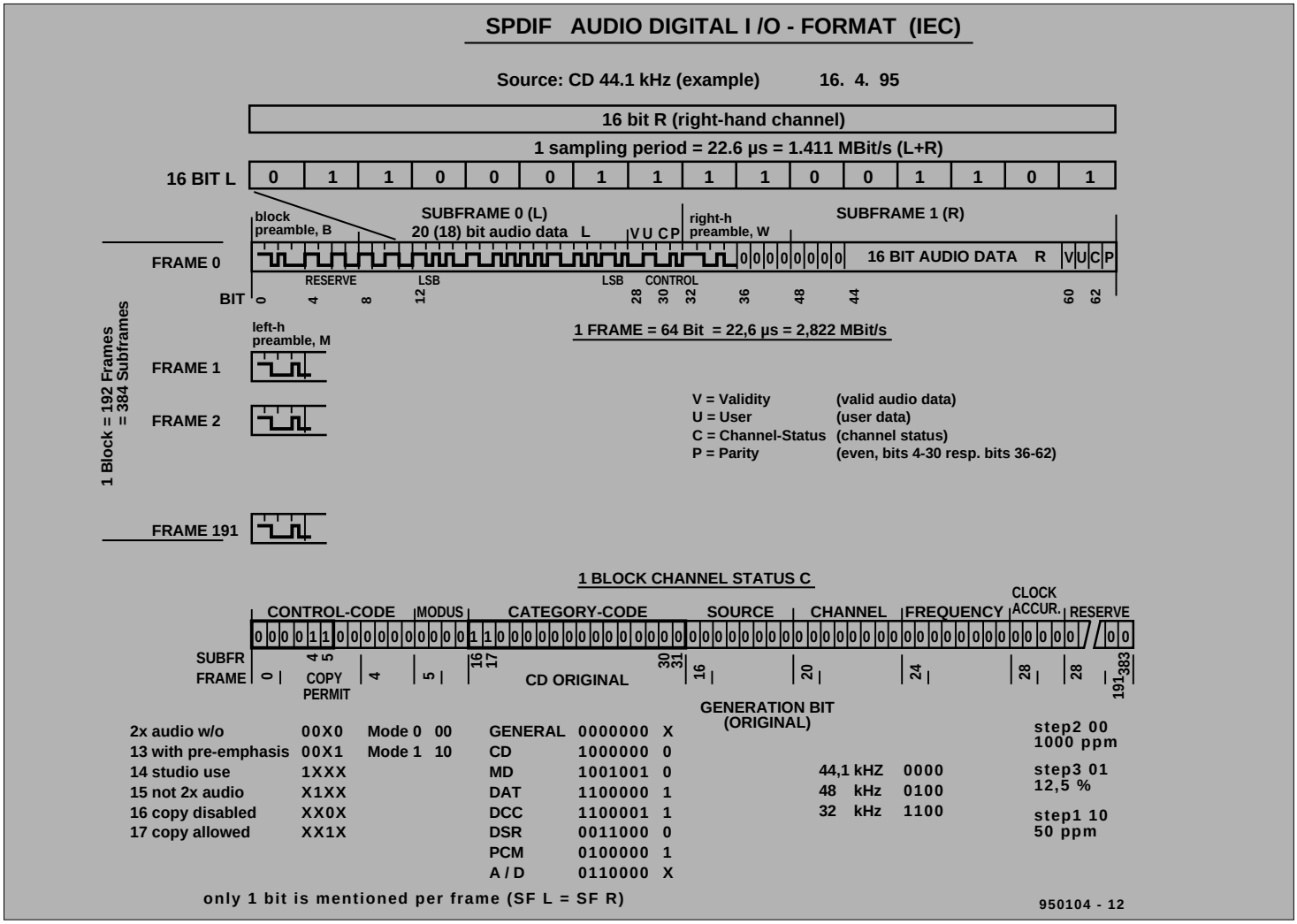


Fig. 2. Composition of a digital audio signal.

about 240 ns, to retrieve the bit clock. In the range of the preambles, the start spacings are >350 ns. This is made use of by retriggerable monostable IC_{3b}, which has a mono time of around 420 ns, to generate the subframe clock. The X-coded XOR pulse occurs only with the block preamble at the first pulse of the subframe clock. This enables the block clock to be decoded.

The block clock is generated regularly when the circuit operates as specified, that is, when there is a digital input signal in S/PDIF format, and the dwell times of the monostables are in accord. The block clock is stretched to a constant-1 signal (NOINV) by IC_{1d} and IC_{1e}; its presence is indicated by D_{10}. If, for instance, the signal has an incorrect frequency, NOINV prevents it being modified and this is indicated by D_{10} lighting less brightly. The LED does not light at all when the input signal is not of the S/PDIF format.

To count the subframes, a 9-bit counter is timed by the subframe clock and reset by the block clock. The 5-bit counter for the subframe bits is in synchrony with the bit clock and is reset by the subframe clock.

Filtering the desired bits (bit 30 in subframes 4, 5, and 16–31) is effected by programmable IC_2. The INVERT pulse has the correct position when signal IN_1 is delayed by about 60 ns (IN_2). A logic 1 is indicated when the relevant LED is driven by the level detector signal output by IC_2. This signal is generated in a manner similar to that of the block clock. Each D-bistable associated with a given LED is reset by the block clock and set with the 1-signal. The period to the next reset is long enough to enable the LED indicating the 1 in a stable way (without flickering).

Inversion of the bit is accomplished by an XOR gate and the 354 ns long INVERT pulse that is located half-way between the C-bit and P-bit—see Fig. 6. The change from 0 to 1 presents no difficulties, since the edges of the INVERT pulse in signal IN_{12} meet at the centre of the bit at equal levels. Short spurious pulses at the centre of the bit can, however, not be avoided entirely. This does not matter, however, since the biphase-modulated signal is always sampled at the centre of a bit-cell, that is, at 1/3 and 2/3 of the bit.

When bit C_8 and C_9 in the input signal are logic 1 (magnetic tape drive), they will not be affected. All other signal sources are assigned the code of a CD player.

Moreover, bits 0 and 1 of the channel status are held at logic 0. Although this is

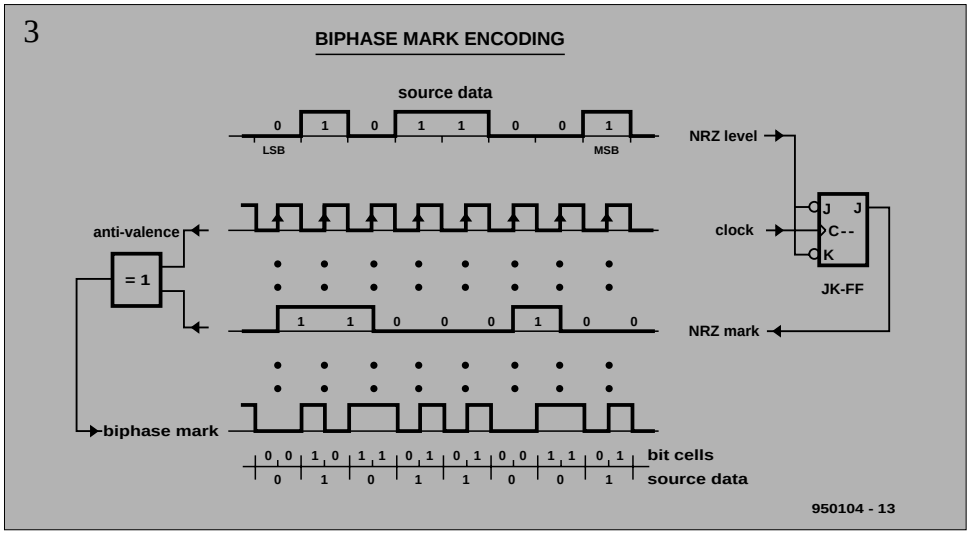
LED indications

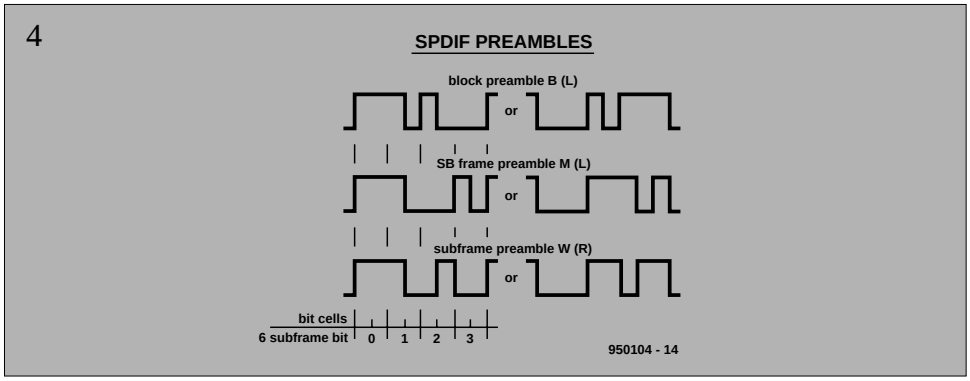
•. Only D_9 lights in both switch positions: ready for use; no S/PDIF

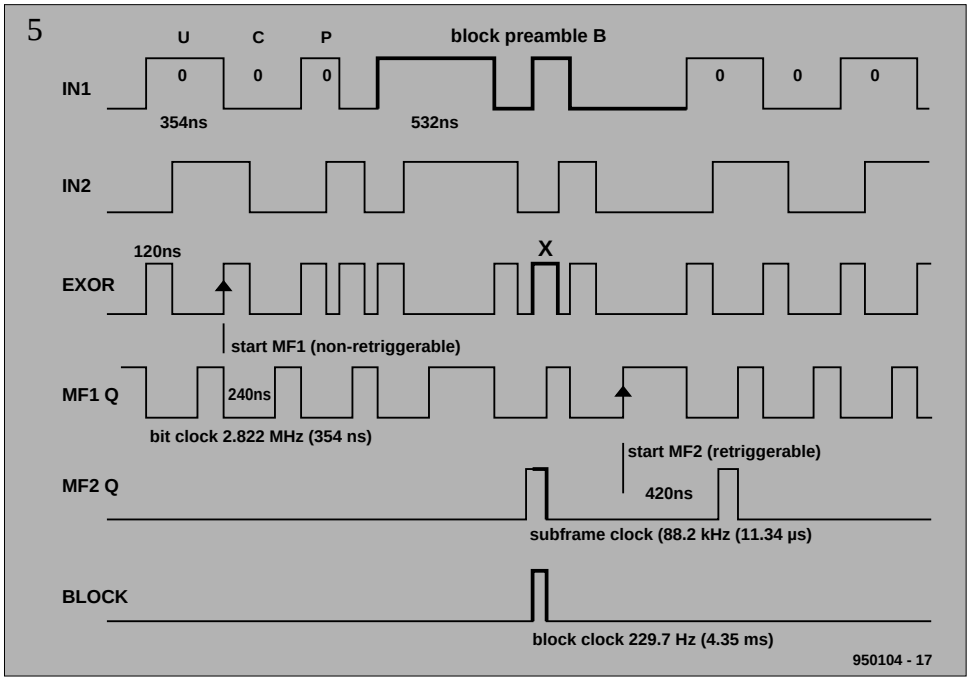
• LEDs flicker: unit is not operating correctly. It may be that both inputs are used simultaneously, or that the input signal is not of the correct format, or that the setup is incorrect, or that the optical input receives spurious signals.

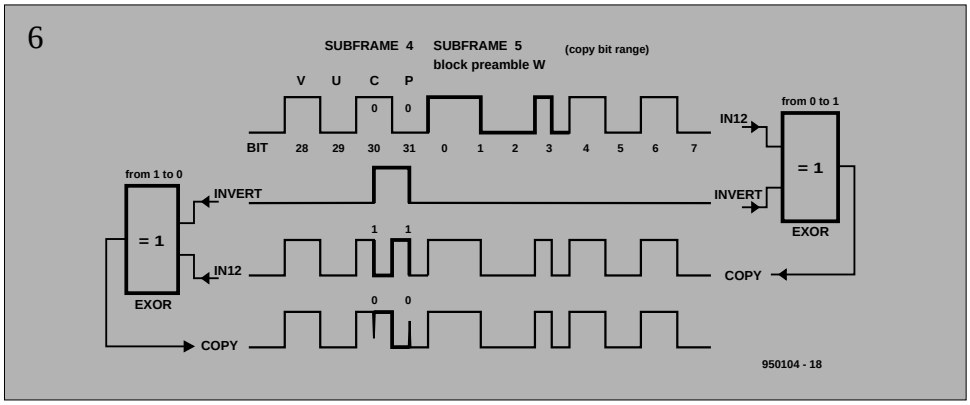
•. D_9 and D_{10} do not light: unit functions as converter; S/PDIF signal is transferred unchanged.

•. D_{10} lights brightly: the S/PDIF input signal, with copybit and category, is indicated The output signal is DAT when the input comes from a magnetic tape drive, and CD when comes from any other source. In both cases, copying is permitted.









not really necessary in domestic equipment (since the bits then are always logic 0), it makes it possible for professional recordings or other recordings marked by these bits (which are inhibited) to be copied—but see warning at beginning of this article.

With switch S_1 open, the inverter accepts sampling frequencies of 44.1 kHz and 48 kHz, but with 32 kHz it must be closed to alter the time constants of the monostables. If this switch is in the wrong position, D_9 and dimly lit D_{10} indicate that the signal is unchanged: the unit functions as a converter. A no-signal condition is indicated by D_9 lighting.

It is highly improbable that only the generation bit, which does not count in the equipment coding, is encoded. Anyway, there is always D_{10} as a controlling element.

The output is buffered by inverter IC_{1f}. Resistors R_4 and R_5 lower the signal level to about 0.5 V_{pp} into 75 Ω. Capacitor C_1 blocks any direct voltage.

Timing the monostables

Construction of the inverter on the printed-circuit board in Fig. 9 should not present any undue difficulties. All ICs, except IC_6, should be seated in sockets. Be careful with inserting IC_2 into its PLCC socket. Do not forget the wire bridge underneath IC_2.

After the board has been finished and thoroughly checked, set the presets to the centre of their travel.

Apply an audio signal, preferably from a CD player set to PAUSE (which ensures a very stable signal) to the coaxial input socket. Set switch S_1 to 44.1/48 kHz, whereupon D_3 (category code CD) should light. If an oscilloscope or logic analyser is not available, adjust presets P_1, P_2 and P_3 (in that order) on to the centre of the stable LED indication.

With S_1 in position 32 kHz, the signal source must be a DAT recorder, set to the long-play analogue recording mode, or a DSR tuner. Carefully readjust P_3 (which should not be much) and recheck the settings with a signal from a CD player. For most practical purposes, these settings are fine.

If more accurate settings of the presets are required, an oscilloscope is needed. Apply an a.f. signal at a level of 0.5 V_{pp} to the coaxial, not to the optical, input. Set the oscilloscope time base to 100 ns cm^{-1}

Fig. 3. Biphase coding enables the simultaneous transmission of the audio signal and the clock.

Fig. 4. Various waveforms of a non-biphase coded preamble.

Fig. 5. Extraction of the bit-clock, subframe clock and block clock.

Fig. 6. Principle of bit inversion.

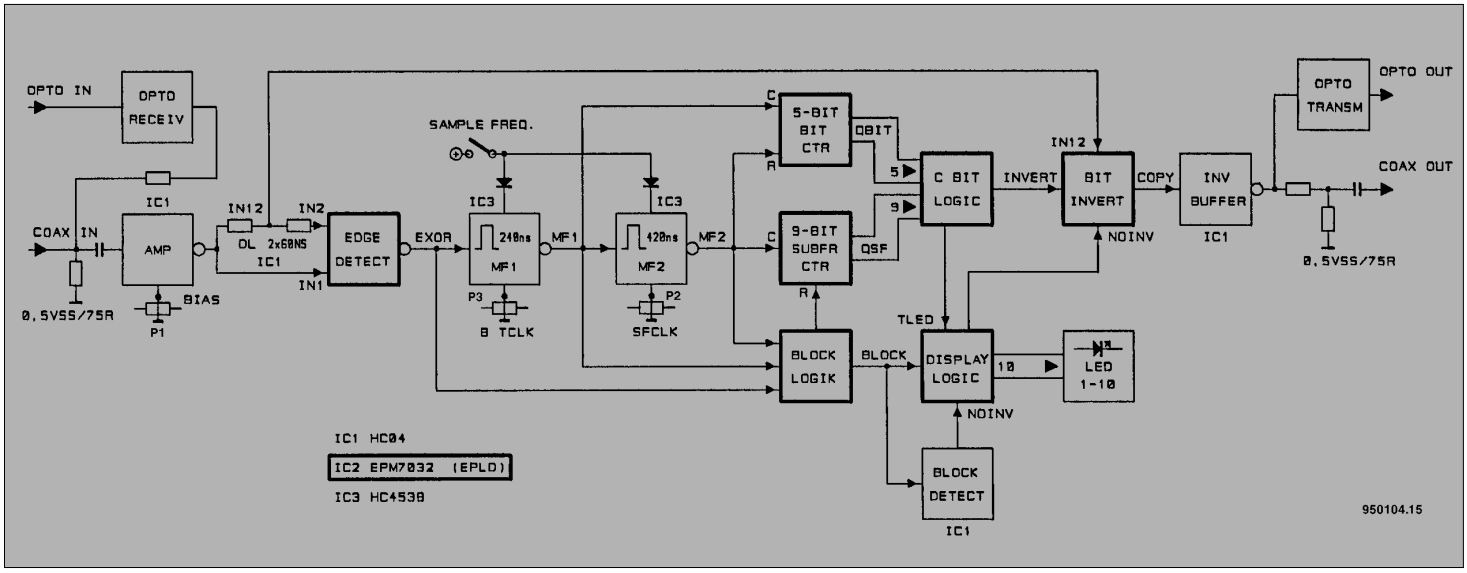


Fig. 7. Block diagram of the copybit inverter.

and connect the instrument to pin 9 of IC_3. Adjust P_1 so that all edges cover one another as well as possible. This ensures that the operating point of the unit is centralized and that the delay of the rising edge of signal IN_2 is equal to that of the trailing edge.

With P_2, set the pulse width of the subframe clock at pin 7 of IC_3 to 100–150 ns. If there is an appreciable difference in dwell times between the standard and long-play settings, the value of R_{12} may be adapted accordingly.

If the oscilloscope has a second time base or *x*-multiplier ×10, the copybit (bit 30) corrected to logic 1 in subframe 4 or 5

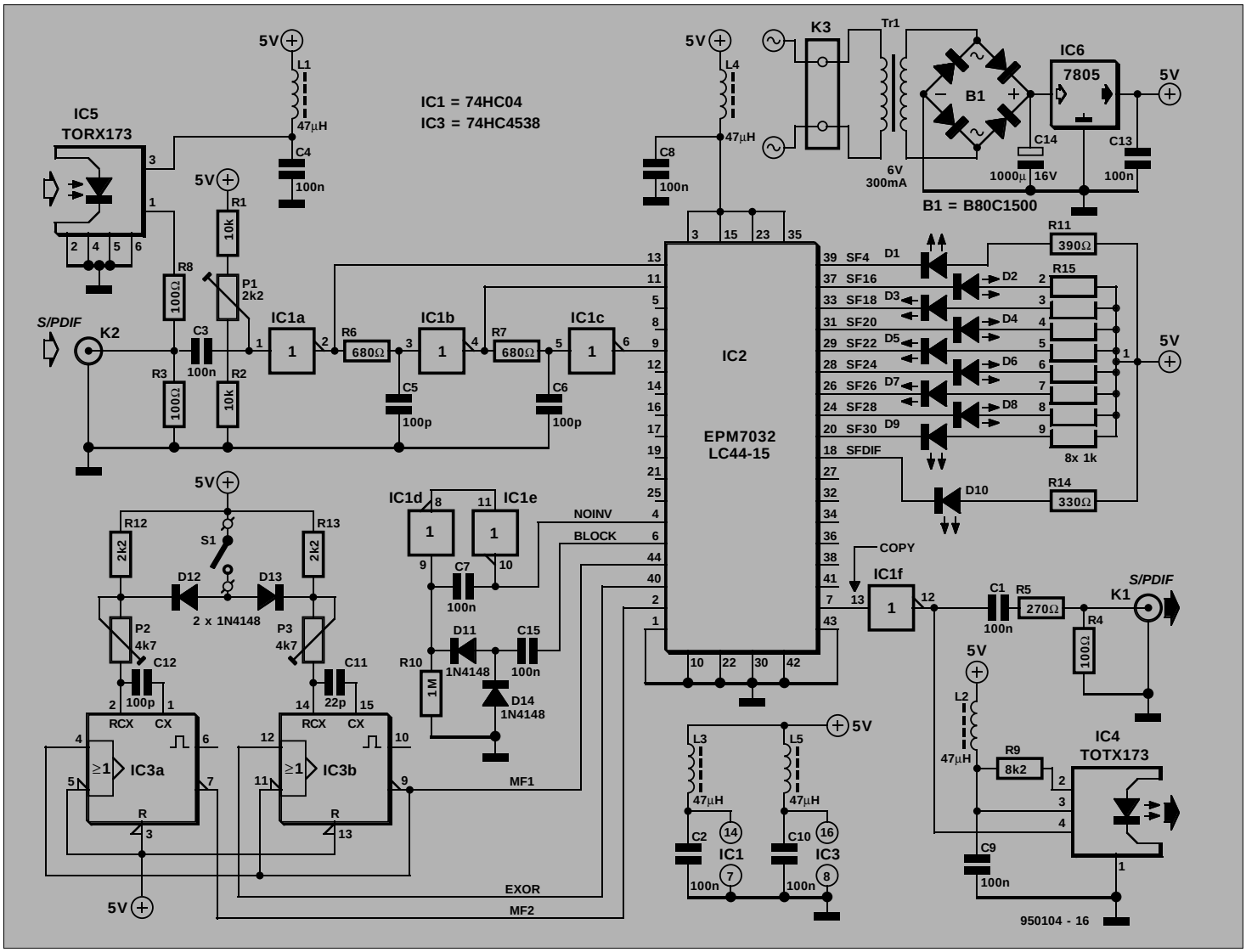


Fig. 8. Circuit diagram of the copybit inverter.

can be timed in the output signal with P_3 [time base set to 10 (1) µs cm^{-1} and triggering to start the block at the leading edge of the cathode signal of a lighted LED (D_1–D_9)].

The high and low level portions of the C-bit set to logic 1 should be equal or very nearly so. If the P-bit is inverted from logic 0 to 1, it should be virtually undistorted.

If the bits away from the block start are to be checked, the LED voltage (trigger at trailing edge) associated with the P-bit can be used for marking them.

During the setting up, make sure that the LEDs light over a fairly wide range. Appreciable differences can be negated by adapting the value of R_{13}.

As a final check, record the output of the copybit inverter on a DAT or DCC recorder. Some DAT recorders show the ID6: this must be 00 both during recording and subsequent playback of the recording—see Fig. 1. Make sure that D_1 lights as an indication that the unit has correctly inverted and processed the input signal.

Parts list

Resistors:
R_1, R_2 = 10 kΩ
R_3, R_4, R_8 = 100 Ω
R_5 = 270 Ω
R_6, R_7 = 680 Ω
R_9 = 8.2 kΩ
R_{10} = 1 MΩ
R_{11} = 390 Ω
R_{12}, R_{13} = 2.2 kΩ
R_{14} = 330 Ω
R_{15} = resistor array, 8.1 kΩ
P_1 = preset, 2.2 kΩ
P_2, P_3 = preset, 4.7 kΩ

Capacitors:
C_1–C_4, C_7–C_{10}, C_{13}, C_{15} = 100 nF, ceramic
C_5, C_6, C_{12} = 100 pF
C_{11} = 22 pF
C_{14} = 1000 µF, 16 V, vertical

Semiconductors:
D_1, D_{10} = LED, low-current, 3 mm, green
D_2–D_9 = LED, low-current, 3 mm, red
D_{11}–D_{14} = 1N4148

Integrated circuits:
IC_1 = 74HC04
IC_2 = EPM7032LC44-15 (Altera), programmed with software 956513-1*
IC_3 = 74HC4538
IC_4 = TOTX173 (Toshiba)
IC_5 = TORX173 (Toshiba)
IC_6 = 7805

Miscellaneous:
K_1, K_2 = audio socket for board mounting
K_3 = 2-way spring-loaded terminals for board mounting, pitch 7.5 mm
S_1 = toggle switch with on contact
B_1 = B80C1500, round
Tr_1 = mains transformer, 6 V, 300 mA
44-pin PLCC socket for IC_2
Enclosure 120×40×70 mm

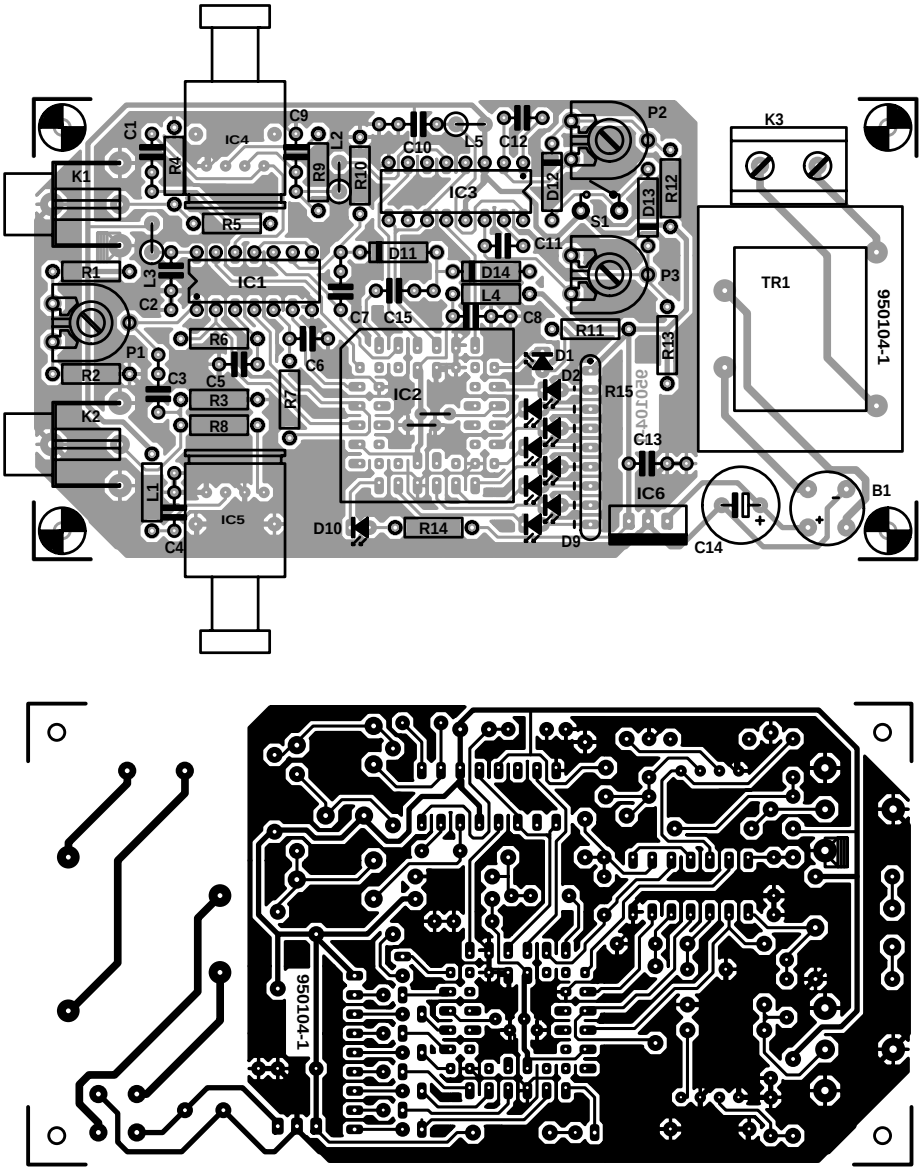


Fig. 9. Printed-circuit board for the copybit inverter (scale 1:1).

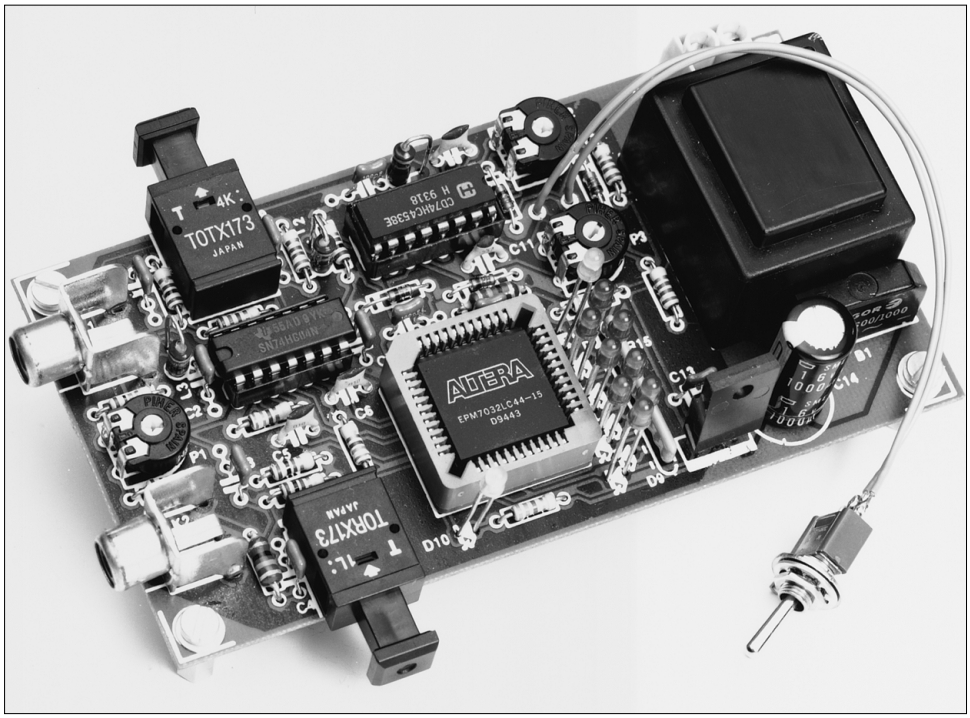


Fig. 10. Finished prototype board.

When a digital-to-analogue converter (DAC) is used in conjunction with a CD player, their clocks must be in synchrony to make sure that the DAC can process the data error-free. In practice, this means that the clock of the CD player has to be applied to the DAC.

If the DAC is built into the CD player, the CD player clock can be applied as shown in the upper diagram. The clock signal is available at TTL level at the output of IC_{1b}. The DAC clock, IC_{2a}, is synchronized with IC_{1a} via P_1 and C_6. In practice, P_1 is set just past the point where synchrony commences: this ensures that oscillator IC_2 continues to work when IC_{1a} is disabled for whatever reason.

An important advantage of the design is that the circuit does not influence the operation of the electronics in the CD player (which thus retains its original functionality).

If the DAC is used as a stand-alone unit, a transmission line for the data and clock signals is required. As usual, this is a 75 Ω coaxial cable. The lower diagram shows how this setup can be arranged.

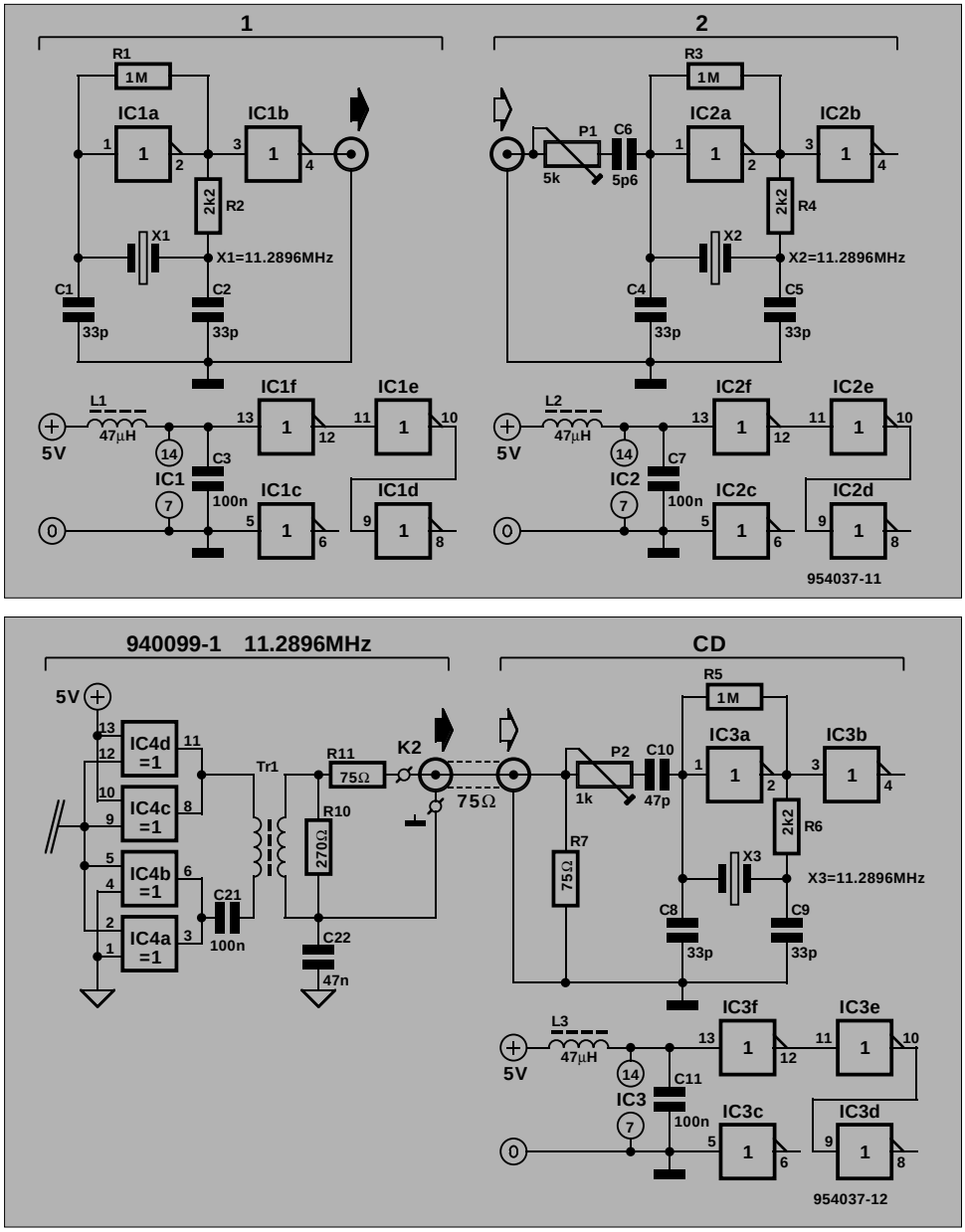
The chosen signal level of 1.5 V_{pp} is more than sufficient to ensure synchrony. The values of coupling components P_2 and C_{10} are, however, different from those of P_1 and C_6 in the upper diagram.

A drawback of this setup is that the oscillator no longer starts spontaneously owing to the increased damping. Fortunately, this can be remedied readily. Resistor R_6 limits the energy transferred from the buffer amplifier to the crystal. If the value of this resistor is greatly reduced, even down to 0 (wire bridge), it will be found that the oscillator starts spontaneously again. Note that in some CD players R_6 is replaced by a wire bridge.

Another remedy is reducing the turns ratio of the transformer, which increases the level of the clock signal. If this is done, the value of P_2 can be increased an that of C_{10} reduced. The load on the oscillator is then smaller, so that it starts spontaneously,

The oscillator circuit draws a current of about 10 mA.

Design by T. Giesberts



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PCB Order no. 950104*

* Combination packet Order no. 950104C

Sources:
Sony SCMS Handbook DTC-55ES

Valvo TI871011

DIN EN 60 968

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