sampling rate converter

for compatibility in digital audio

Although there are still dyed-in-the-wool sound technicians who swear by the good old analogue recording technology, most others, bitten by the digital audio recording bug, do not want to revert to analogue recording. They have experienced the pleasures of loss-free processing and copying of recordings at digital level. These pleasures turn to frustration, however, when they want to convert a **DAT** recording on to a **CD**. This cannot be done just like that because the two have different sampling frequencies: **DAT** 48 kHz, and **CD** 44.1 kHz. To overcome this difficulty, a converter as described in this article is required.

Design by T. Giesberts

It is a regrettable fact, with which we will have to learn to live, that different audio techniques use incongruous sampling frequencies (**CDI** – 18.9 kHz; 8 mm **VCR** – 31.5 kHz; **NICAM** – 32 kHz; **CDI** – 37.8 kHz; **VCR** – 44.056 kHz; **CD** – 44.1 kHz; **DAT** – 48 kHz; and others).

The growing popularity of digital audio is creating an increasing need of some means of coupling equipment using such different techniques – without loss of quality, of course. This can be done by altering the sampling rate in one of the two units to be coupled, while ensuring that the two sampled signals are adequately synchronized. Clearly, this requires a well-designed intelligent converter.

The design of the present converter is based on a dedicated **IC**: the Type TDA1373H from Philips. This circuit is very versatile and may be used for almost any imaginable conversion (but not quite – see later). Thus, it can be used for converting a **DAT** recording into a **CD** recording. Also, it enables **CD** data to be recorded on a **DAT** machine with a sampling rate of only 32 kHz, which, of course, results in a much longer playing time. Another possibility is converting the consumer standard **S/PDIF*** to the professional **AES/EBU*** format. True, the converter has no **AES/EBU** connectors, but the conversion is possible.

Apart from as a converter, the circuit may be used as a copybit eliminator. In that case, the two sampling rates are made equal (as in the converter), but the category code, the copybit and the generation-status bit are set. The sampling rate used must correspond with the code set in most DAT machines to ensure that the signal is accepted.

Finally, the circuit may also serve as jitter killer since the first-in-first-out (**FIFO**) and gain stage in the TDA1373H suppresses any jitter.

DESIGN

The circuit of the converter is shown in the diagram of **Figure 1**. Circuit IC_1 is the integrated digital converter, IC_2 is the controller, and IC_3 is the output interface.

The most important property of the TDA373H is the integrated Audio Digital Input Circuit (**ADIC**), which enables the chip to decode IEC958 signals (**S/PDIF** or **AES/EBU**). The circuit can work on a stand-alone basis or be controlled by a microprocessor. In the present circuit, it is controlled by IC_2, since this gives a wider choice of output formats. The circuit can process up to 20 bits and afterwards provides the con-

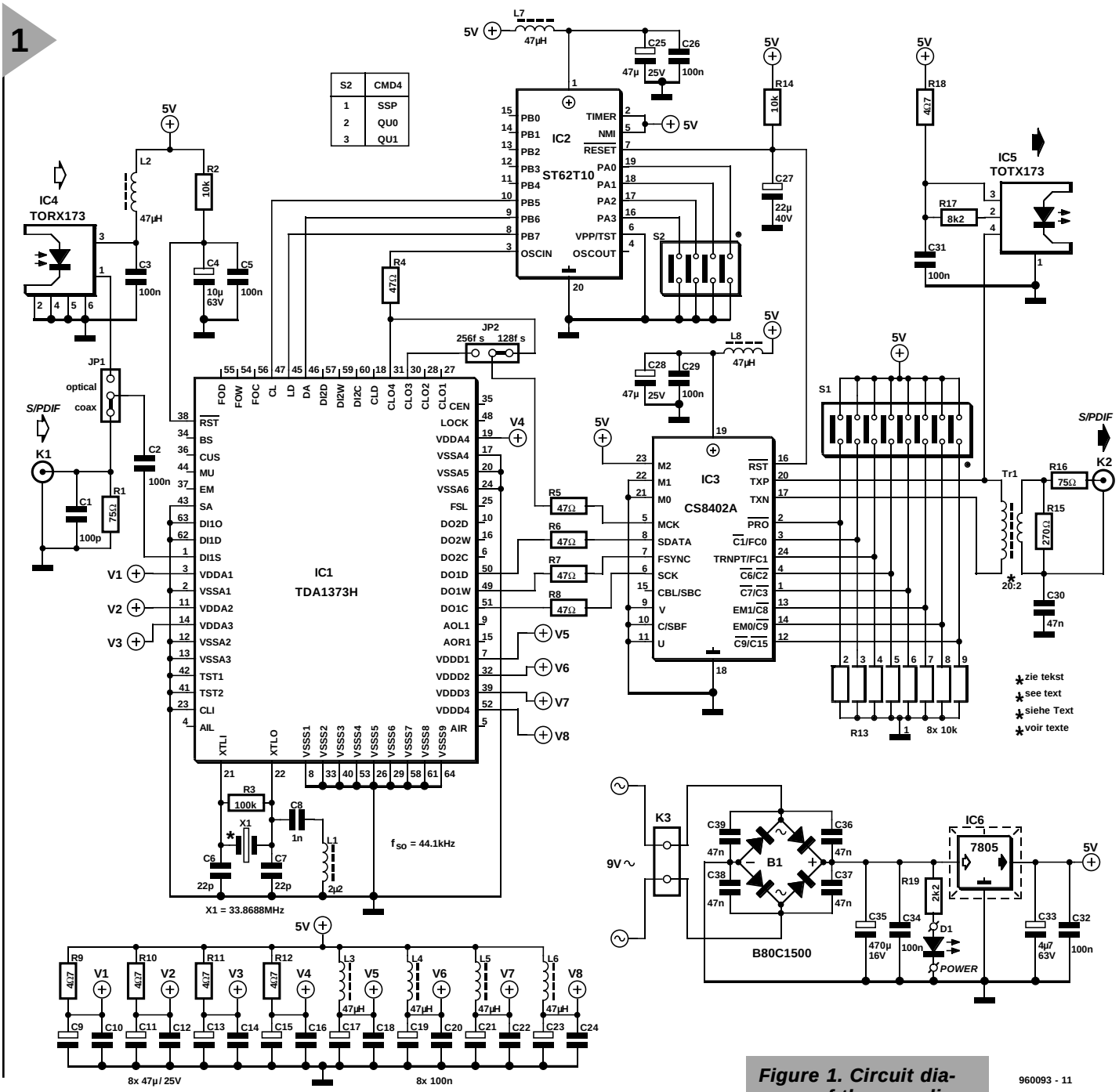

Figure 1. Circuit diagram of the sampling rate converter in which IC_1 is the actual converter, IC_2 is the controller, and IC_3 is the output interface.

verted data in 16-, 18-, or 20-bit format.

The TDA373H is designed to provide up to four different applications, but since the present circuit is geared to being used as a sampling rate converter, the circuit is limited to this application.

The input of the converter may be optical (via IC_4) or coaxial (via K_1). The selection between these two is by jumper JP_1, since it is assumed that the converter will be used invariably in a fixed setup in which there is seldom or never a need for changing from one to the other. The remaining two input pins of IC_1 are linked to earth.

Correct operation of IC_1 requires the setting of six command registers, which is effected by controller IC_2.

After a brief power-up reset (by R_{14}-C_{27}), IC_2 sends twelve 8-bit words (six addresses and data) to IC_1 via a serial connection.

The in-band noise shaper and the stop-band suppression of the ×64

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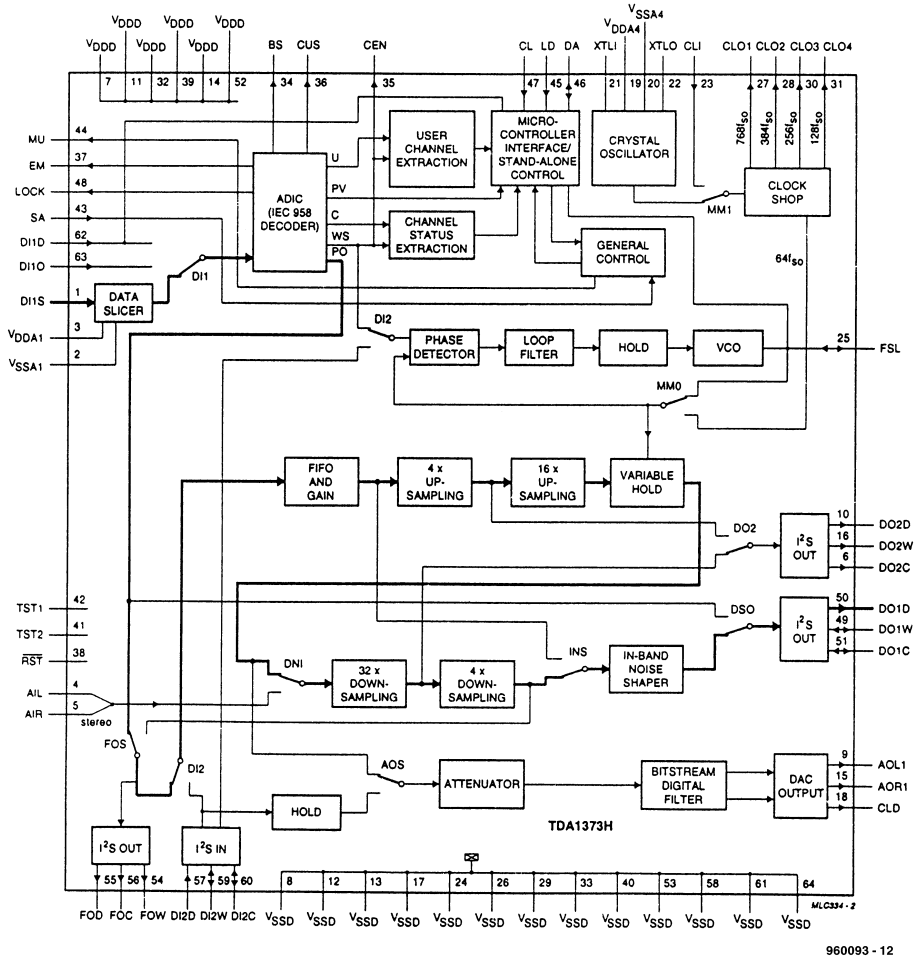

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Figure 2. IC_1 affords various functions. The relevant signal paths for the sampling rate conversion are indicated by bold lines.

oversampling filter are set by, respectively, sections 2, 3 and 1 of quadruple **DIP** switch S_2. The switches are debounced by a delay of 1–1½ seconds between their being operated and the relevant function being actuated. This delay is effected by the controller.

The sampling rate of the output signal, $f_{s(o)}$, of IC_1 is determined by the crystal between pins 21 and 22, according to equation

$$f_{x1} = 768 f_{s(o)}.$$

Thus, the crystal frequency should be 33.8688 MHz for a sampling rate of 44.1 kHz, and 24.576 MHz for a sampling rate of 32 kHz.

The sampling rate of the input, $f_{s(i)}$, must be not lower than $0.35\, f_{s(o)}$, nor higher than $1.45\, f_{s(o)}$. Thus, if the circuit is used as IEC598 decoder only, the input sampling rate should not exceed 45 kHz if the output sampling rate is 32 kHz. If conversion from 48 kHz to 32 kHz is required, consideration should be given to using two converters in cascade.

The converted data are available at serial digital audio output 1 and applied to output interface IC_3 via resistors R_6–R_8, which provide di/d*t* limiting.

Circuit IC_3 is a digital audio interface transmitter Type CS8402. This IC can also process various formats, but in the present circuit the serial input (pins, 6, 7 and 8) is fixed for I^2S by the levels at inputs M0, M1 and M2. Virtually all functions of IC_3 may be obtained by appropriate setting of the various sections of DIP switch S_1.

The symmetrical output at **TXP**, **TXN**. is converted into a standard **S/PDIF** output (0.5 V_{pp} into 75 Ω). The electrical isolation provided by the transformer has the benefit of preventing earth loops.

An optical output is provided by optoisolator IC_5.

The power supply may be based on a standard 9 V mains transformer or mains adaptor rated at not less than 300 mA. The supply lines are stabilized by regulator IC_6 and lavishly decoupled as shown in the diagram.

THE TDA1373H

The TDA1373H, called general digital input, is a circuit that provides four different modes of operation. However, the present application is that of sampling rate converter, **SRC**, and, therefore, only the parts relevant to this will be discussed in this section.

In the block diagram in **Figure 2** the relevant signal paths are shown in bold lines.

The input signal is applied to the data slicer via pin DI1S. The slicer can handle signals at levels from 200 mV_{pp} to 5 V_{pp}.

The output of the slicer is applied to the audio digital input circuit, **ADIC**, which decodes the stereo audio samples, the word clock, the bit clock and various data (**V**, **U**, **C** and **P**) bits. The last function is not used here.

The **ADIC** locks to a 44.1 kHz signal in not more than 1 ms. Until it has locked, there is no word clock, and the audio bits are muted.

The output of the **ADIC** is applied to

Table 1. Two different response curves of the x64 oversampling filter can be selected with section 1 of DIP switch S_2.

S2-1:				
bit SS	*pass band*		*stop band*	
0	*0–0.45351$f_{s(i)}$*	*±0.004 dB*	*0.54648–1$f_{s(i)}$*	*–70 dB*
1	*0–0.46875$f_{s(i)}$*	*±0.004 dB*	*0.53125–1$f_{s(i)}$*	*–50 dB*

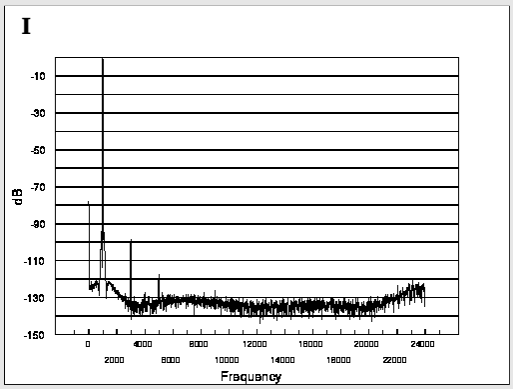
Test results

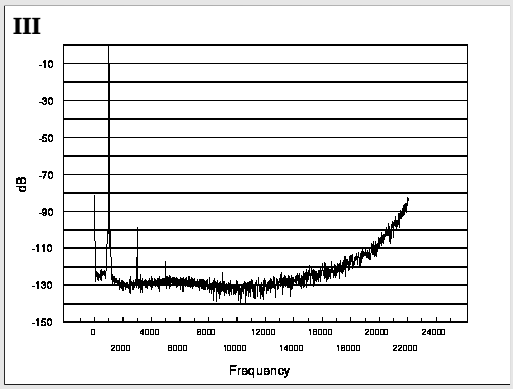
The quality and properties of the sampling rate converter were tested in the digital domain at the various output formats. The (analogue) generator of an Audio Precision Analyser was used as the digital signal source, and this was coupled to a 20-bit analogue-to-digital converter (ADC). Of the four characteristics shown, I represents the output spectrum of the ADC. The other three characteristics may be compared with this.

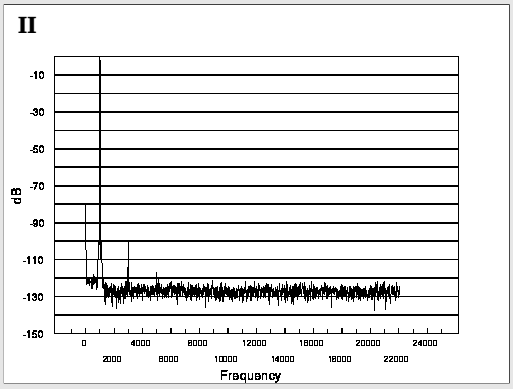
Note how well the action of the in-band noise shaper is seen in Characteristic IV; a clear rise is discernible only in the (virtually inaudible) range above 18 kHz.

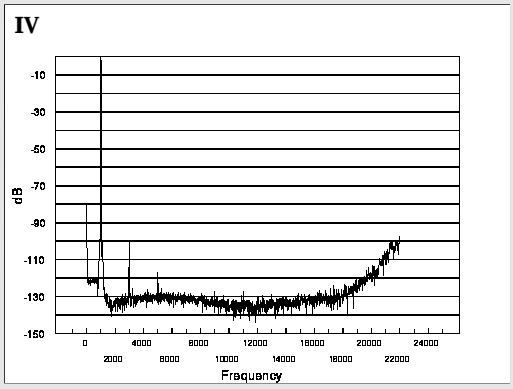
At the same time, and with the same setup, the signal-to-noise ratio for the various output formats was determined:

- *16 bit rounded off: –94.5 dB;*
- *16 bit INS: –89.7 dB;*
- *18 bit INS: –95.5 dB;*









- *II: 16 bit rounded off (section 2 of S_2 on; section 3 of S_2 on).*
- *III: 16 bit INS (section 2 of S_2 on; section 3 of S_2 off).*
- *IV: 18 bit INS (section 2 of S_2 off; section 3 of S_2 off).*

No characteristic is shown for the 20-bit mode (section 2 of S_2 off; section 3 of S_2 on), since, at least up to 20 kHz, this is all but identical to the input signal of the converter (Characteristic I).

- *20 bit: –97 dB.*

Note that the signal-to-distortion ratio of the ADC was 97.5 dB (measured without noise).

The signal-to-noise of the ADC plus sampling rate converter (without distortion) in the same test setup was about –107 dB (dynamic range of the ADC). The dynamic range, measured at a digital-to-analogue converter, DAC, was about 5 dB better with 16 bit INS than with 16 bit rounded off.

the first-in-first-out, **FIFO**, and gain stage. The **FIFO** section equalizes any speed variations of the incoming samples. Its size is eight samples and it ensures a tracking speed of 4 kHz ms^{-1}.

The gain section enables the signal to be amplified or attenuated. In the present application, the signal is attenuated by 0.068 dB to prevent clipping in the digital filters.

The samples are fed for interpolation to a ×64 oversampling filter. This filter consists of a ×4 section and a ×16 section. There is a choice of two filter characteristics: one with

Table 2. The word-lenght of the samples may be adapted with section 2 and 3 of DIP switch S_2.

S_2-2:	S_2-3:	
bit QU0	bit QU1	lenght of word
0	0	16 bit (rounded off)
1	0	20 bit
0	1	16 bit INS
1	1	18 bit INS

a stop-band suppression of 70 dB and the other with a stop-band suppression of 50 dB but with steeper skirts. The second is intended especially for use with signals with a sampling rate of 32 kHz, and a pass-band of 0–15 kHz as, for instance, in digital satellite radio. The characteristics are selected by section 1 of DIP switch S_2 – see also **Table 1**.

The samples are applied from the filter to the variable hold stage in which the actual sampling rate conversion takes place. Depending on the ratio of the input sampling rate and the output sampling rate, the sample is used once or twice, whence the name variable hold. When the ratio is 1:1, all samples are used twice, since the down sampling is ×128.

The variable hold function is controlled by a digital phase-locked loop, **PLL**, formed by the phase detector, loop filter, hold, and **VCO** (voltage-controlled oscillator) stages.

The loop filter ensures that the **PLL** locks rapidly. This is necessary because, after power-up, the bandwidth of the filter is reduced in two steps from 500 Hz to 50 Hz and then from 50 Hz to 0.5 Hz. The frequency difference is only 1 Hz for 512 input samples (10 ms for a sampling rate of 44.1 kHz).

After the **PLL** has locked in, the audio signals are demuted and the conversion commences. To prevent any errors, the **FIFO** is monitored continuously in the variable-hold phase. As soon as the slightest tracking error is detected, the bandwidth of the loop filter is enlarged.

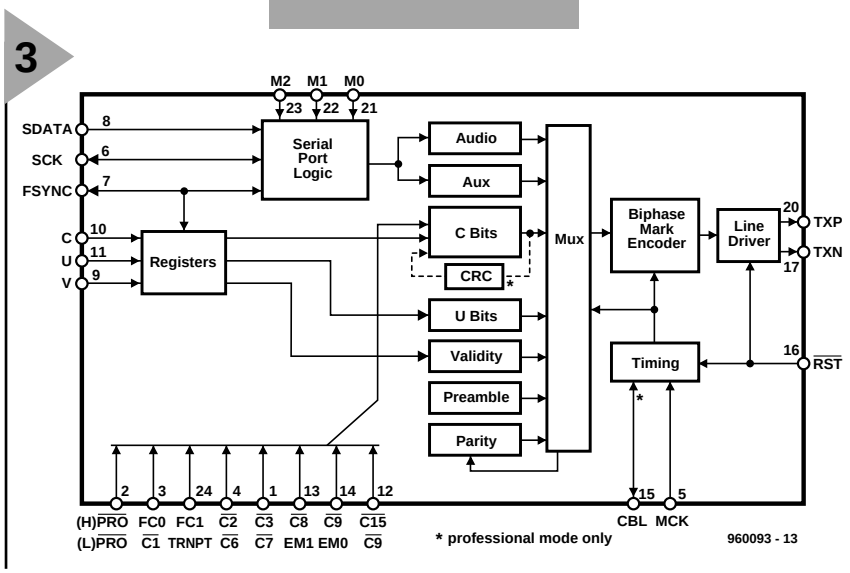
To convert the sampling rate to the requisite output value, the samples are passed through a ×128 down-sampling filter, which consists of a ×32 section and a ×4 section. The overall filter provides a stop-band suppression of 80 dB from 0.54648 of the output sampling rate.

Finally, the samples are applied to an in-band noise shaper, **INS**, which adapts the word-length of the samples to specific requirements. The standard length of 20 bits may be reduced to 16 bits or 18 bits by the relevant sections of **DIP** switch S_2. There are four possibilities as enumerated in **Table 2**, the first of which is 20 bits.

The **INS** has a facility for adapting the digitization noise in a psycho-acoustical manner, whereby the noise to which human hearing is most sensitive is shifted upwards in frequency. This facility gives a subjective improvement of two bits with respect to the real quantization level.

Finally, the 20 bit length may be reduced to a 16-bit length by a simple rounding off action.

Figure 3. IC_3 is a digital audio interface transmitter intended to encode and send audio data in accordance with the usual standards.



usual interface standards. The circuit provides the possibility of setting the most important channel status bits via seven inputs: pins 3, 24, 4, 1, 13, 14 and 12 in **Figure 3**. These inputs are controlled by octal **DIP** switch S_1 (see Figure 1). All seven inputs have a double function, which depends on the level at pin 2. This level is set with section 8 of S_1 and determines whether the IC works in the professional (**AES/EBU**) or in the consumer (**S/PDIF**) mode. The audio data are coded to the standard associated with the selected mode.

In the professional mode, a **CRC** code may be generated (channel status byte 23) as shown in dashed lines.

The serial input, pins 6, 7 and 8, can handle seven different formats and audio samples of 16–24 bits. In the present circuit, the format is fixed for I^2S with M0, M1 and M2.

The serial inputs for channel status, **C**, user data, **U**, and validity, **V**, are not used and linked to earth. The **V** bit must be low to indicate that audio data are being processed which can be converted to analogue signals.

Pin 15, channel block start, **CBL**, is not used in the present application either. Normally, it is an output that may be used for writing **C**, **U** and **V** bits. CBL is an input only when in the professional mode the transparent option is chosen (in which the **C**, **U** and **V** bits can be looped in via a receiver). In this way, synchronization of signals coming from separate equipment is possible. Normally, the master clock, MCK, is 128 f_s, where f_s is the signal frequency, but in the transparent mode, MCK = 256 f_s. The multiplier is set with jumper JP_2.

Table 3a. Sampling rates in professional mode.

S_1-8:	S_1-5:	S_1-4:	
PRO	C6	C7	
0	0	0	not defined
0	0	1	48 kHz
0	1	0	44.1 kHz
0	1	1	32 kHz

CODING & CONTROL

The digital audio interface transmitter, IC_3, is intended primarily for coding and sending audio data according to

PROFESSIONAL MODE

When pin 2, $\overline{PRO}$, is low, that is, when section 8 of S_1 is closed, the digital audio interface transmitter, IC_3, is in the professional mode. In this mode, bits 1, 2, 3, 4, 6, 7 and 9 may be set after a 1 has been sent for channel status bit 0.

C0 indicates whether the channel status block applies to the professional (1) or the consumer (0) mode.

C1 determines whether the data are audio (0 – section 6 of S_1 closed) or

Table 3b. Sampling rates in consumer mode.

S_1-8:	S_1-6:	S_1-7:	
PRO	FC1	FC0	
1	0	0	44.1 kHz
1	0	1	48 kHz
1	1	0	32 kHz
1	1	1	44.1 kHz, CD-mode

not audio (1 – section 6 of S_1 open).

C2, C3 and C4 are coded by EM0 (section 2 of S_1) and EM1 (section 3 of S_1) and determine the emphasis to be used: for instance, 110 is 50/15 µs.

C6 and C7 determine the sampling rate. The requisite setting of the relevant sections of S_1 is given in **Table 3a**.

Table 4. Setting the category code.

S_1-8:	S_1-3:	S_1-2:	
PRO	C8	C9	
1	0	0	general format
1	0	1	PCM-encoder/decoder
1	1	0	CD
1	1	1	DAT

A 1 at C9 (section 2 of S_1 open) indicates a stereo signal; a 0 means that the mode is indeterminate.

In the transparent mode, none of the stated pins is used: the channel code is read at the **C** input only.

CONSUMER MODE

When pin 2, **PRO**, is high (section 8 of S_1 open), the digital audio interface transmitter is in the **S/PDIF** (consumer) mode. In this mode, bits 2, 3, 8, 9, 15, 24 and 25 may be set after a 0 has been sent for channel status bit 0.

C0 – 0 – indicates that the channel status block applies to the consumer mode.

FC0 and FC1 determine the sampling rate. The requisite setting of the relevant sections of S_1 is given in **Table 3b**.

C2 gives a choice between copy prohibit (0 – section 5 of S_1 closed) or copy permit (1 – section 5 of S_1 open).

C3 determines whether emphasis (50/15 µs) will be applied (1 – section 4 of S_1 open) or not (0 – section 4 of S_1 closed).

C8 and C9 determine the category code: the requisite setting of the relevant sections of S_1 is shown in **Table 4**.

C15 is the generation status bit. Depending on the category code, the function of this bit, determined by the setting of section 1 of S_1, is inverted. When the category code is 001xxxx, 0111xxx or 100xxxx, a 0 indicates that the bit is an original and a 1 that it is a copy. With all other category codes, the reverse is true.

When the copy bit is 1, there is no copy protection, so that copying is possible. If the copy bit is 0, the generation status bit, in combination with the category code, determines whether copying may be carried out or not.

The outputs of IC_3 are RS422 compatible line drivers that go low when the IC is being reset.

Make sure that the channel status bits are active low and that a 0 is set by closing the relevant section of the DIP switch.

CONSTRUCTION

The converter is best built on the printed-circuit board shown in **Figure 4**. Although the board is compact, it affords ample space for all parts and components, including audio sockets K_1 and K_2 and optoisolators IC_4 and IC_5. It does not have space for the mains transformer, however. Note that controller IC_2 is available ready programmed through our Readers services (see towards the end of this issue).

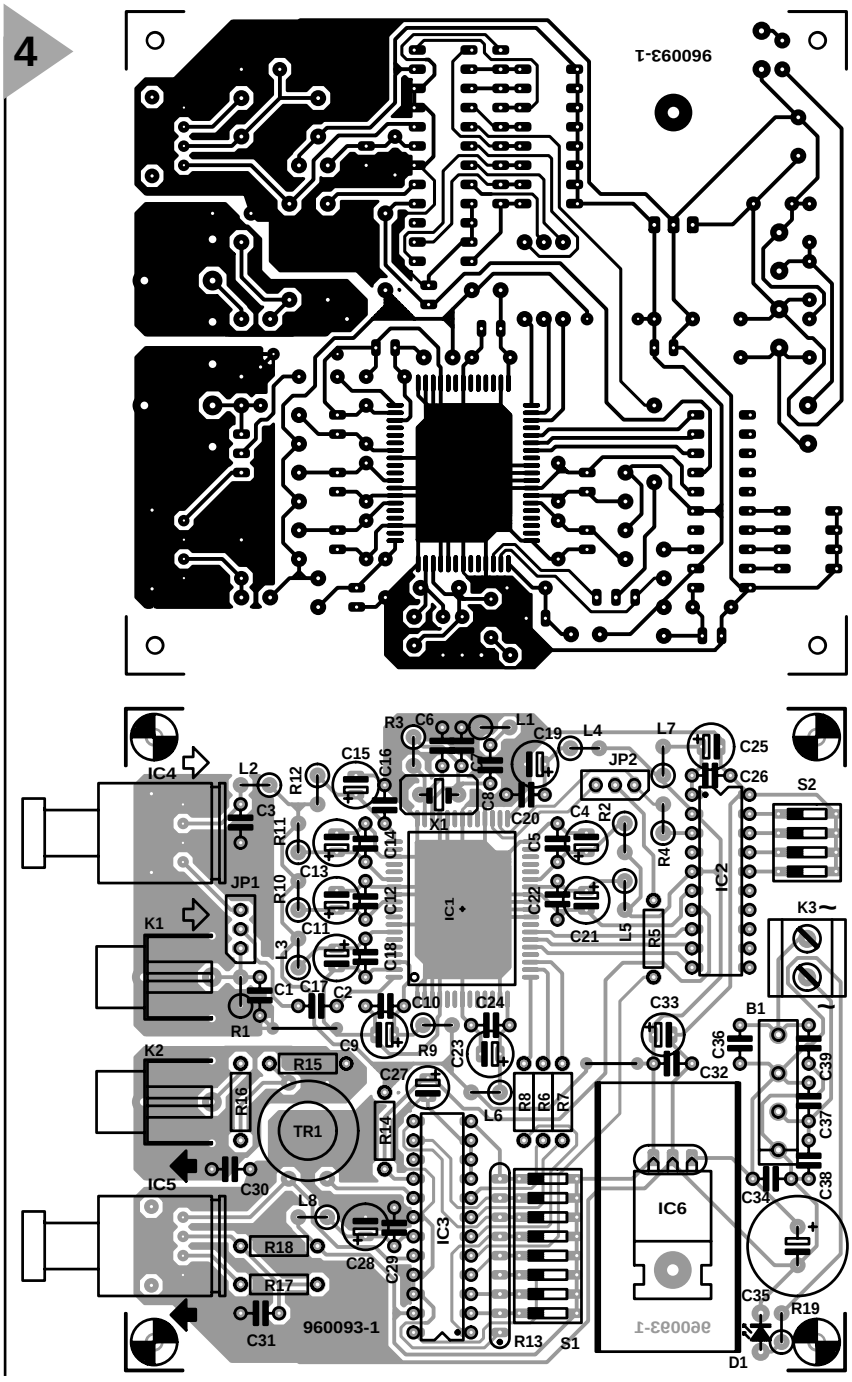


Figure 4. Printed-circuit board for the sampling rate converter. Note that IC_1, a surface-mount device, must be soldered at the track side.

PARTS LIST

Resistors:
R_1, R_{16} = 75 Ω
R_2, R_{14} = 10 kΩ
R_3 = 100 kΩ
R_4–R_8 = 47 Ω
R_9–R_{12}, R_{18} = 4.7 Ω
R_{13} = 8×10 kΩ array
R_{15} = 270 Ω
R_{17} = 8.2 kΩ
R_{19} = 2.2 kΩ

Capacitors:
C_1 = 100 pF
C_2, C_3, C_5, C_{10}, C_{12}, C_{14}, C_{16}, C_{18}, C_{20}, C_{22}, C_{24}, C_{26}, C_{29}, C_{31}, C_{32}, C_{34} = 100 nF ceramic
C_4 = 10 µF, 63 V, radial
C_6, C_7 = 22 pF
C_8 = 1 nF ceramic
C_9, C_{11}, C_{13}, C_{15}, C_{17}, C_{19}, C_{21}, C_{23}, C_{25}, C_{28} = 47 µF, 25 V, radial
C_{27} = 22 µF, 40 V, radial
C_{30}, C_{36}–C_{39} = 47 nF, ceramic
C_{33} = 4.7 µF, 63 V, radial
C_{35} = 470 µF, 16 V, radial

Inductors:
L_1 = 2.2 µH
L_2–L_8 = 47 µH

Semiconductors:
D_1 = LED, low current

Integrated circuits:
IC_1 = TDA1373H (Philips)
IC_2 = ST6210 (see Readers services)
IC_3 = CS8402A (Crystal)
IC_4 = TORX173 (Toshiba)
IC_5 = TOTX173 (Toshiba)
IC_6 = 7805

Miscellaneous:
JP_1, JP_2 = 3-way pin header and jumper
K_1, K_2 = audio socket for board mounting
K_3 = terminal block, pitch 5 mm
S_1 = octal DIP switch
S_2 = quadruple DIP switch
Tr_1 = wound on G2/3FT12 core - see text
B_1 = rectifier Type B80C1500
X_1 = see text
Heat sink for IC_6: 29 k W^{-1}, for instance, Fischer ICK35/SA, available from Dau, telephone 01243 553 031)
PCB Order no. 960093 (see Readers services)
Mains transformer or mains adaptor, 9 V, 300 mA

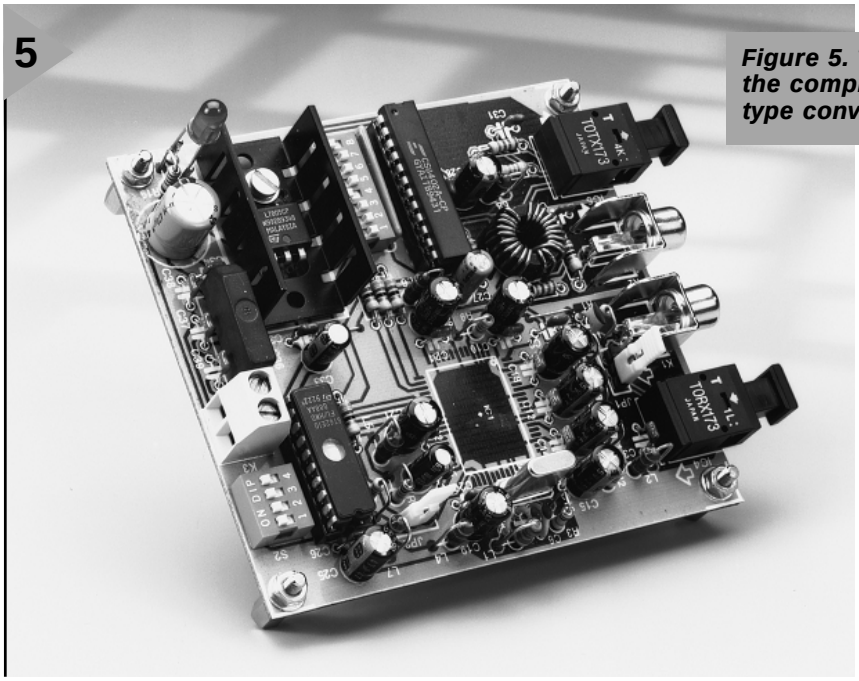


Figure 5. Top view of the completed prototype converter board.

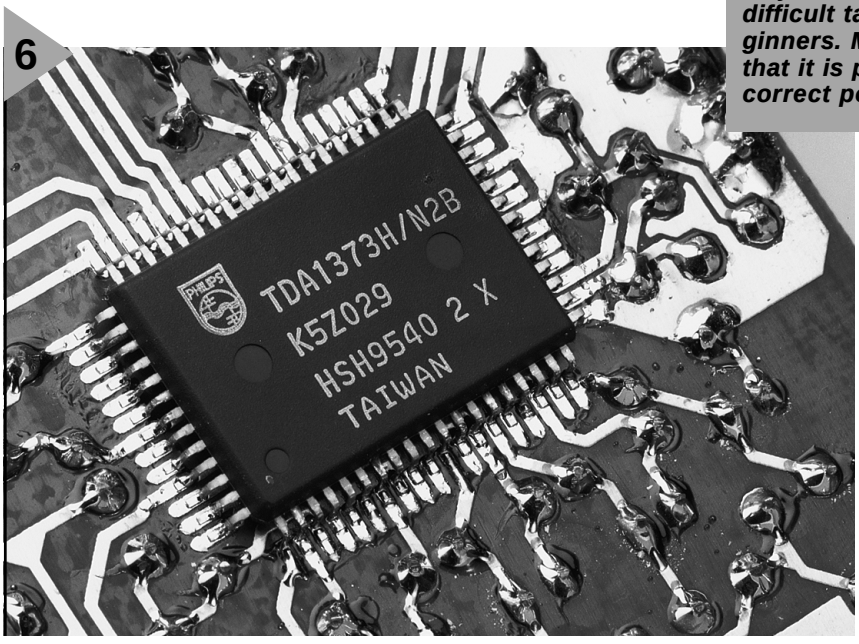


Figure 6. Mounting IC_1 may be a somewhat difficult task for beginners. Make sure that it is placed in the correct position.

The completion of the board should not present any undue difficulties – see **Figure 5** for a view of the top of a completed board. Note that IC_6 is mounted on an appropriate heat sink.

Less experienced constructors may find the mounting of IC_1 and the construction of output transformer Tr_1 not so straightforward.

Circuit IC_1 is a surface-mount device, SMD, which should be soldered at the track side (underside) of the board using an iron with a very fine tip – see **Figure 6**. Note the correct way of fitting: pin 1 is identified by a small disk on the case: this side must point towards the connectors on the board.

Transformer Tr_1 is a DIY device which is wound on a G2/3FT12 core. The primary winding consists of 20 turns, and the secondary of two turns, of enamelled copper wire with a diameter of 0.7 mm.(SWG22). Spread the primary evenly across the core, but leave some space at the centre for the two secondary turns that have to be wound subsequently.

When the board has been completed and checked thoroughly, a suitable mains transformer (9 V, 300 mA) or a 9 V mains adaptor may be connected to K_3. Indicator D_1 should then light.

Using a multimeter, check whether a stable potential of 5 V exists across C_{32} and C_{33}. If so, it is virtually certain that the converter will work satisfactorily. If it does not, recheck the board thoroughly. It is not possible to give suitable test points, since all that can really be checked are the supply lines.

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