delay line

The delay line makes possible an improvement of the surround-sound decoder published in this magazine in early 1995*.

The differential signal of the surround-sound channel is first passed through a low-pass filter and then split into two. Whereas IC_{1c} functions as a buffer, IC_{1b} inverts the signal. Both signals are then applied to identical memories of the bucket-brigade type.

Circuits IC_3 and IC_4 are controlled synchronously by IC_5. The delayed signals are buffered by IC_{2a} and IC_{2d}, after which they are applied to differential amplifier IC_{2c}. As the signals are in antiphase, the output of IC_{2c} is twice the level of each, so that the ripple caused by IC_5 is reduced appreciably (since the interfering signals are in phase).

The remaining interference signals at the output of IC_{2c} are inevitable, because they are related to the large tolerances of the memories.

According to data from the manufacturers, the distortion of an MN3008 is 0.5 per cent (average) and 2.5 per cent (maximum), while the amplification may vary up to ±4 dB from the nominal value. In the prototype, the use of one memory resulted in a distortion of 06–0.8 per cent at 1 kHz When two memories are used, the distortion drops to below 0.1 per cent. In both measurements, the clock frequency of IC_5 was 40 kHz (25 ms delay).

The improvement of the present circuit over the original is particularly noticeable with strong signals, because the signal-to-noise ratio increases to 63 dB.

The performance may improved even further by matching MN3008s. In the prototype, this reduced the distortion to 0.04 per cent. However, the price of the ICs may prove prohibitive for most constructors.

Another way of improving the performance is providing input buffers IC_{1b} and IC_{1c} with an offset compensation control. This requires the availability of a good distortion meter, however.

The bandwidth of the circuit is limited to about 7 kHz by input filter IC_{1a} and output filter IC_{2b}. Probably owing to tolerances of the capacitor values, the bandwidth in the prototype is 6.3 kHz. This is not terribly important, however. If desired, the bandwidth may be increased by giving R_2–R_5 and R_{24}–R_{27} proportionally lower values. Note that the bandwidth must not become larger than one quarter of the clock frequency, because the slope of the filter skirts does not allow this.

The clock frequency of IC_5 may be set between 30 kHz and 100 kHz with P_1. These values correspond to delays of 33 ms and 10 ms respectively.

The delay line draws a current of about 22 mA.

[T. Giesberts -964119]

* February 1995, p. 26