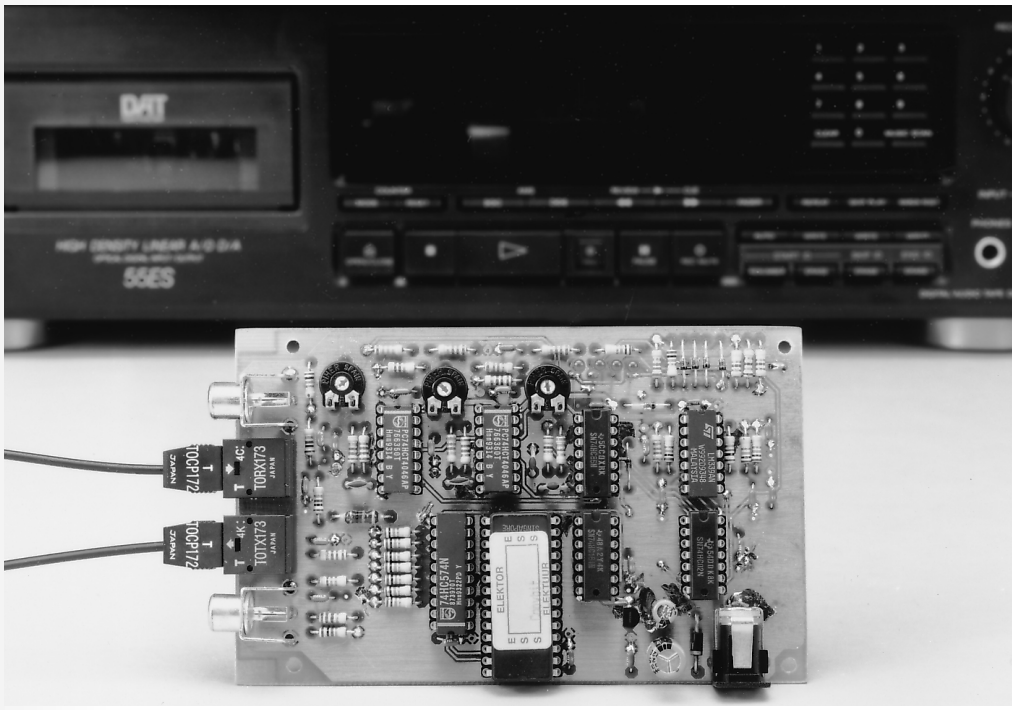
simple copybit killer

enables limitless digital copying

The Serial Copy Management System (SCMS) prevents digital copying of audio material from the second generation onwards. Unfortunately, this protection also works on home recordings and so prevents home recordists from digitally copying their own musical work more than once without degradation by the SCMS. This problem has been highlighted before in this magazine, but it has not gone away – reason enough to describe a simple and inexpensive circuit for permanently removing the copy-prohibit-bit from the S/PDIF* audio signal.



Design by H. Hanft

GENERAL DESCRIPTION

The circuit described in this article is intended for the digital recording or copying and playback of non-commercial musical work. Such recording or copying is possible only when the copy-prohibit has been eliminated without any other effect on the audio signal.

The design of the circuit is such that there are no modifications required in the existing audio installation. The circuit is simply inserted in series with the digital (optical or coaxial) link between the relevant recording and playback equipment.

Briefly, the circuit:

- requires no modification to the digital audio equipment;
- is suitable for use with signals on optical as well as coaxial lines;
- uses readily available components;
- operates without programmable ICs such as PALs and EPLDs;
- is easily set up;
- has good clock regeneration through the use of PLLs (jitterkiller);
- gives clear indication (LEDs) of the sampling frequency (32 kHz, 44.1 kHz, or 48 kHz);
- automatically recognizes, and switches over to, the correct sampling frequency;
- draws a small current owing to the use of CMOS ICs.

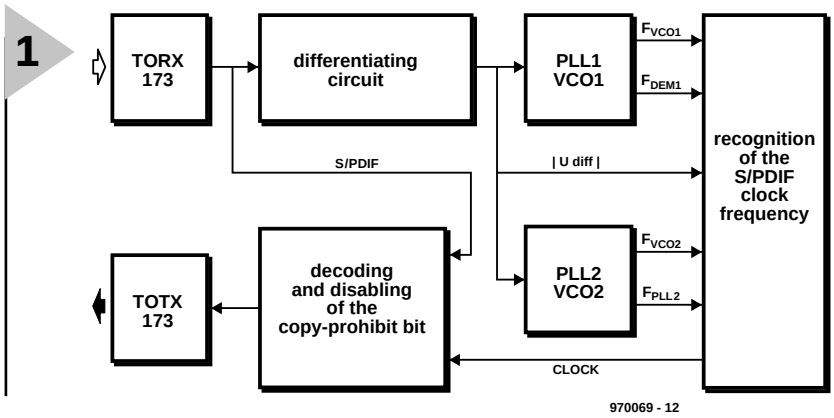
CIRCUIT DESCRIPTION

The block diagram of the copybit killer is shown in **Figure 1**. It shows that the copybit killer consists of:

- optical-to-electrical convertor for the S/PDIF signals;
- differentiating network;
- phase-locked loop (PLL) to regenerate the clock frequency;
- network for recognizing and processing the clock frequency;
- network for recognizing and dis-

** Sony/Philips Digital Interface Format – the consumer version of the AES/EBU standard. This standard was devised by the American Audio Engineering Society and the European Broadcasting Union to define the signal format, electrical characteristics, and connectors, to be used for digital interfaces between professional audio products.*

Figure 1. Block diagram of the copybit killer. The core of the circuit, 'decoding and disabling of the copy-prohibit-bit', uses an EPROM.



abling the copy-prohibit-bit;
- electrical-to-optical convertor for the S/PDIF signals.

The circuit diagram proper is shown in **Figure 2**. The operation of the various networks outlined above is described in the following sections.

The **optical-to-electrical conversion of the S/PDIF signal** is carried out by IC_1, which is the well-known Type TORX173 integrated receiver. It converts the signal input from the fibre-glass cable into an electrical signal at TTL level. There is, of course, also a facility for inputting signals from a standard coaxial cable. This is possible via audio connector K_1 in parallel with the output of IC_1 via resistor R_2.

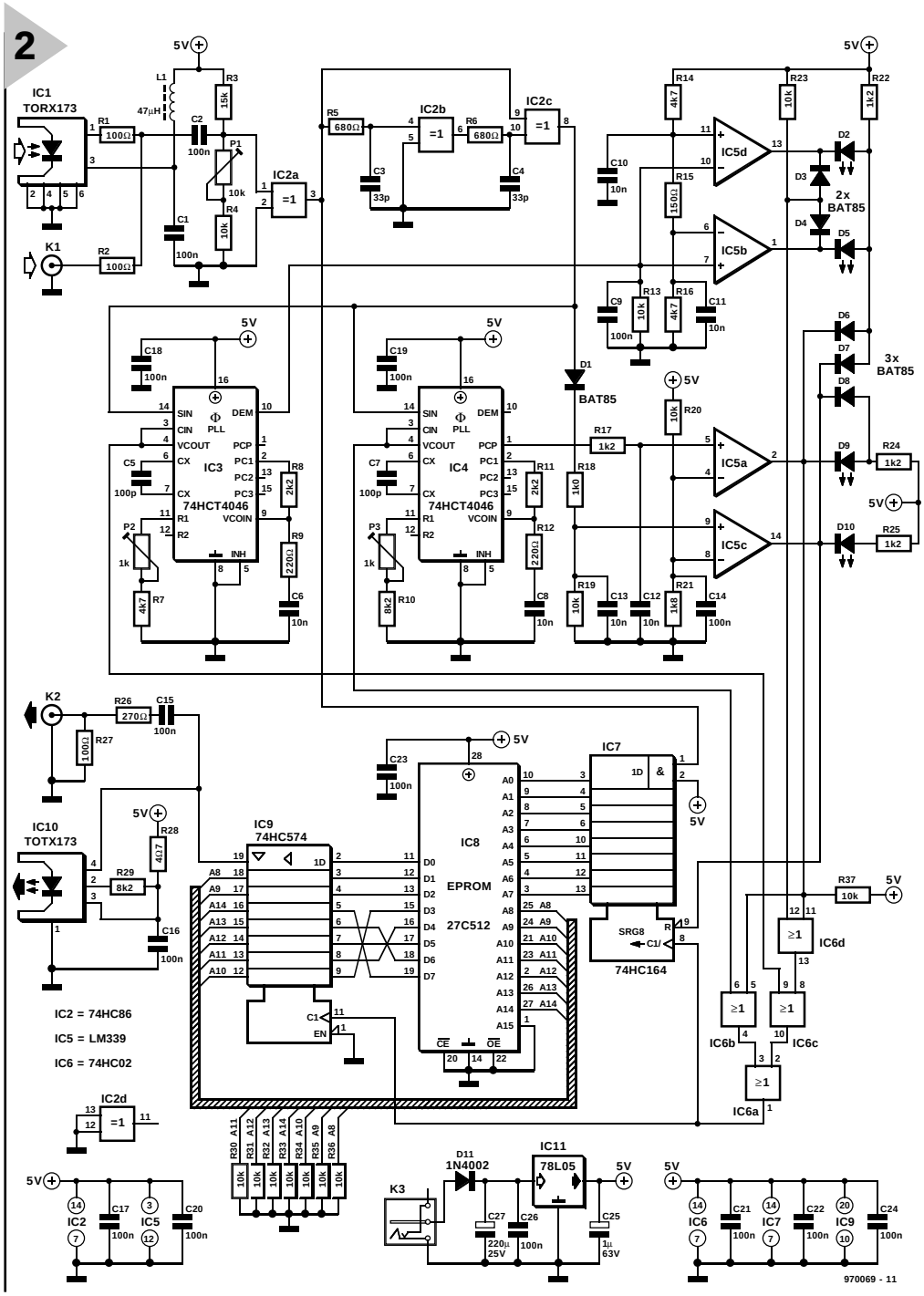
The **differentiating circuit**, consisting of XOR gates IC_{2a}–IC_{2c} and *RC* networks R_5-C_3 and R_6-C_4, serves to detect the rising or falling edges of the incoming S/PDIF signal. For each and every edge, a positive pulse of defined length is generated and used for synchronizing the following PLL.

The regeneration of the clock frequency contained in the S/PDIF signal is carried out by two discrete **phase-locked loops** (PLLs). The first one is for frequencies 6.144 MHz (sampling rate 48 kHz) and 5.6448 MHz (sampling frequency 44.1 kHz), and the second for frequency 4.096 MHz (sampling frequency 32 kHz)

So as to keep the circuit simple, both PLLs are Type 74HCT4046 ICs (IC_3 and IC_4). These circuits contain not only a phase comparator, but also a voltage-controlled oscillator (VCO). The PLLs circuits are virtually identical and differ only as far as the value of the resistor that sets the central frequency of the VCO is concerned (R_7 and R_{10}).

The network for **recognizing the clock frequency** serves to detect the sampling frequency of the S/PDIF signal and pass this on to the decoder. It consists of IC_{5a}–IC_{5d} and four NOR gates, IC_{6a}–IC_{6d}. The comparators recognize the incoming S/PDIF signal and ensure that the PLL locked in at that moment is included in the sigal processing. Also, when the sampling frequency is 48 kHz or 44.1 kHz, the VCO control

Figure 2. Circuit diagram of the copybit killer. All components are readily available and the circuit is easy to build and set up.



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Parts list

Resistors:
R_1, R_2, R_{27} = 100 Ω
R_3 = 15 kΩ
R_4, R_{13}, R_{19}, R_{29}, R_{23}, R_{30}–R_{37} = 10 kΩ
R_5, R_6 = 680 Ω
R_7, R_{14}, R_{16} = 4.7 kΩ
R_8, R_{11} = 2.2 kΩ
R_9, R_{12} = 220 Ω
R_{10}, R_{29} = 8.2 kΩ
R_{15} = 150 Ω
R_{17}, R_{22}, R_{24}, R_{25} = 1.2 kΩ
R_{18} = 1.0 kΩ
R_{21} = 1.8 kΩ
R_{26} = 270 Ω
R_{28} = 4.7 Ω
P_1 = 10 kΩ preset potentiometer
P_2, P_3 = 1 kΩ preset potentiometer

Capacitors:
C_1, C_2, C_9, C_{14}–C_{24}, C_{26} = 0.1 µF, ceramic
C_3, C_4 = 33 pF
C_5, C_7 = 100 pF
C_6, C_8, C_{10}–C_{13} = 0.01 µF
C_{25} = 1 µF, 63 V, radial
C_{27} = 220 µF, 25 V, radial

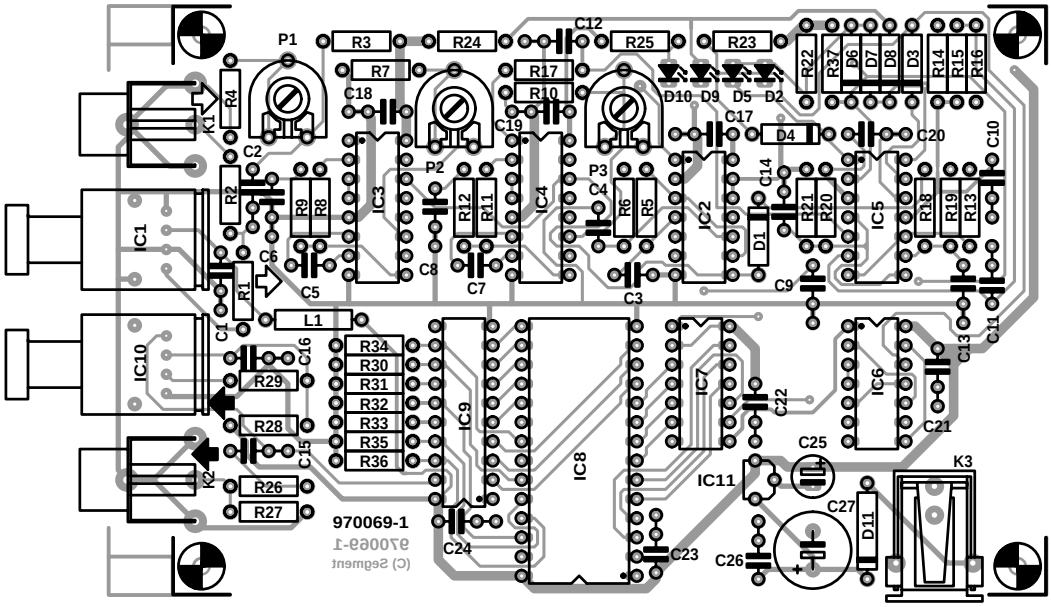
Inductors:
L_1 = 47 µH

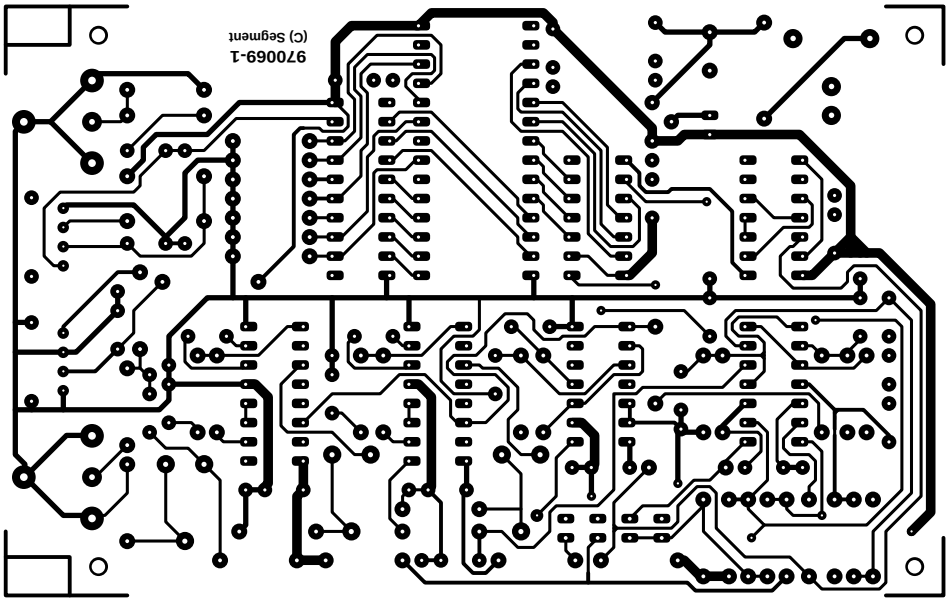
Semiconductors:
D_1, D_3, D_4, D_6–D_8 = BAT85
D_2, D_5, D_9, D_{10} = LED, high efficiency
D_{11} = 1N4002

Integrated circuits:
IC_1 = TORX173
IC_2 = 74HC86
IC_3, IC_4 = 74HCT4046
IC_5 = LM339
IC_6 = 74HC02
IC_7 = 74HC164
IC_8 = 27C512 (available ready programmed: Order no 976516* – see Readers Services towards the end of this issue)
IC_9 = 74HC574
IC_{10} = TOTX173
IC_{11} = 78L05

Miscellaneous:
K_1, K_2 = audio socket for PCB
K_3 = mains adaptor socket for PCB
PCB Order no. 970069* – see Readers Services towards the end of this issue

* These items may be purchased as a combination: Order no. 970069-C





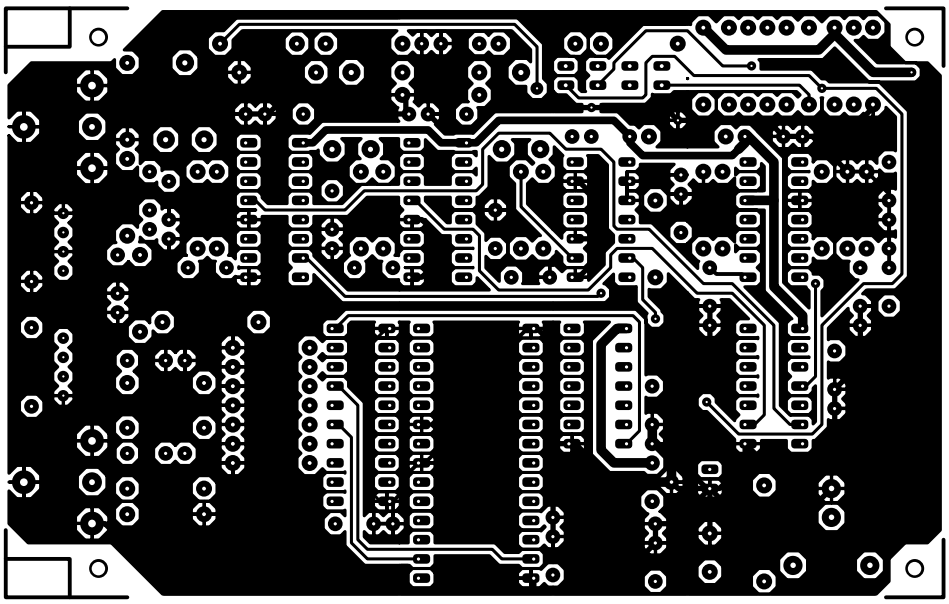
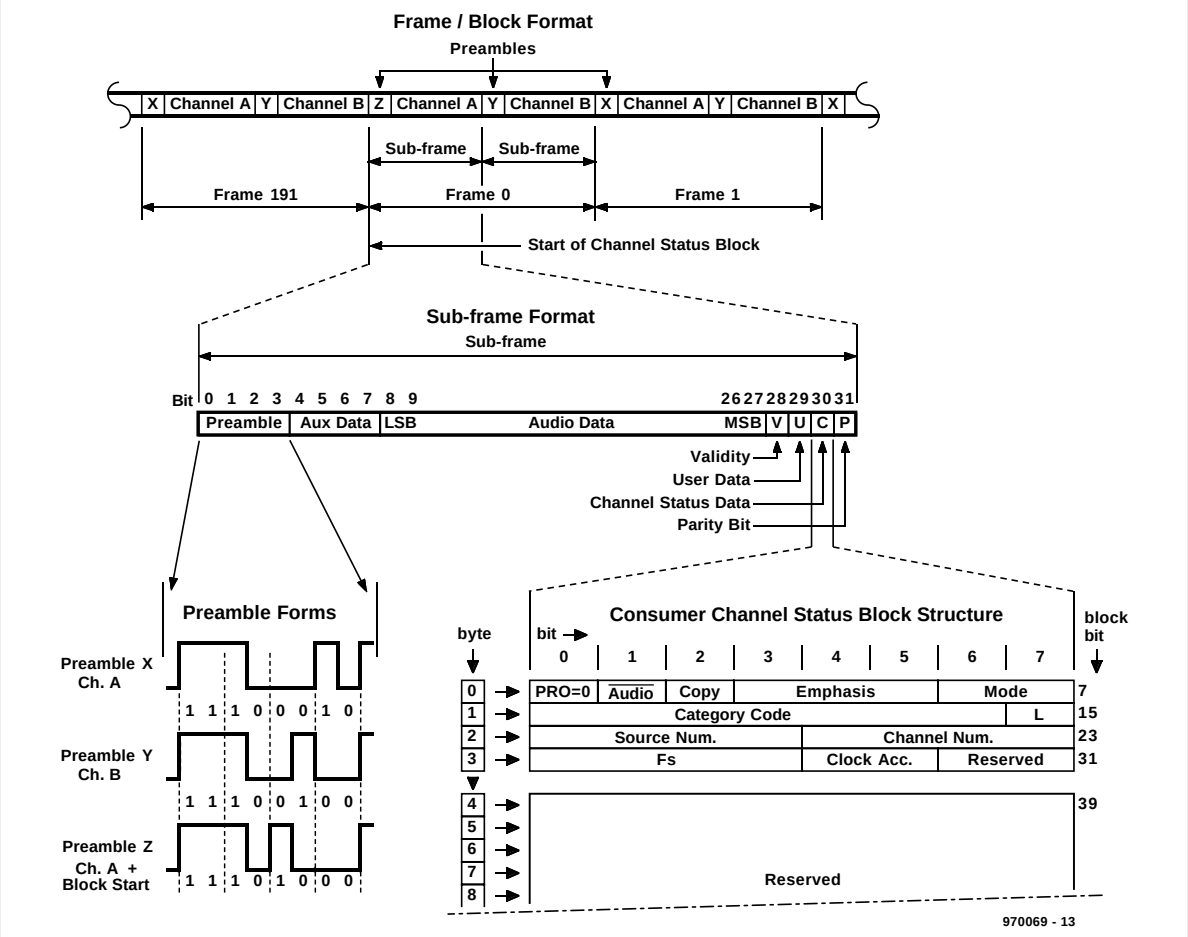


Figure 3. The printed-circuit board for the copybit killer is available ready-made.



Bit management

The digital part of the circuit, in conjunction with the associated programming code in the EPROM, provides a sequence control that recognizes and, if necessary, alters the status of the copy-prohibit-bit. The process attenuation of the S/PDIF signal is equal to one clock cycle. Shift register IC_7 continuously separates the last eight biphase-bit halves from the serial data stream and arranges that the halves are available at A_0–A_7.

The feedback of the data lines to the address lines via latch IC_9 divides the memory of the EPROM into 128 blocks of 256 bytes each. In this way it becomes possible within a block, depending on the status of address lines A_0–A_7, to select the same or another block which is then enabled at the rising edge of the next clock pulse. This arrangement provides processing control in up to 128 steps.

*From the format of the S/PDIF signal in the diagram above, it is seen that a transfer block consists of 192 frames, each of which is composed of two sub-frames. These sub-frames start with a preamble (**X, Y, Z**) and contain 32 bits. The preambles serve to mark the onset of a sub-frame; preamble **Z** also indicates the start of a new transfer block.*

Bit 2 of the Consumer Channel Status Block is of special importance for the present copybit killer, because unlimited digital copying can be carried out only when this bit is set. The Channel Status Bit is located at bit position 30 (biphase-bit-half positions 60 and 61) of a sub-frame and therefore occurs twice during each frame. As far as the copy-prohibit-bit is concerned, these are the sub-frames of frame number 2.

In short, it is necessary that the status of bit number 30 in the two sub-frames of frame 2 be recognized and, if this bit has been erased, that it is set. If one of these bits is altered, the next parity bit (bit position 31) of the sub-frame must be inverted. This may give rise to eight different situations, which have to be taken into account in the programming code in the EPROM—see Table.

	User Data		*Channel Status Data*		*Parity Bit*	
Bit	*29*		*30*		*31*	
Bi-Bit	*58*	*59*	*60*	*61*	*62*	*63*
	*	*	*0*	*0*	*1*	*0*
Case 1	↓	↓	↓	↓	↓	↓
C=0, P=1	*	*	*0*	*1*	*0*	*0*
	*	*	*0*	*0*	*1*	*1*
Case 2	↓	↓	↓	↓	↓	↓
C=0, P=0	*	*	*0*	*1*	*0*	*1*
	*	*	*0*	*1*	*0*	*0*
Case 3	↓	↓	↓	↓	↓	↓
C=1, P=0	*	*	*0*	*1*	*0*	*0*
	*	*	*0*	*1*	*0*	*1*
Case 4	↓	↓	↓	↓	↓	↓
C=1, P=1	*	*	*0*	*1*	*0*	*1*
	*	*	*1*	*0*	*1*	*0*
Case 5	↓	↓	↓	↓	↓	↓
C=1, P=1	*	*	*1*	*0*	*1*	*0*
	*	*	*1*	*0*	*1*	*1*
Case 6	↓	↓	↓	↓	↓	↓
C=1, P=0	*	*	*1*	*0*	*1*	*1*
	*	*	*1*	*1*	*0*	*0*
Case 7	↓	↓	↓	↓	↓	↓
C=0, P=0	*	*	*1*	*0*	*1*	*0*
	*	*	*1*	*1*	*0*	*1*
Case 8	↓	↓	↓	↓	↓	↓
C=0, P=1	*	*	*1*	*0*	*1*	*0*

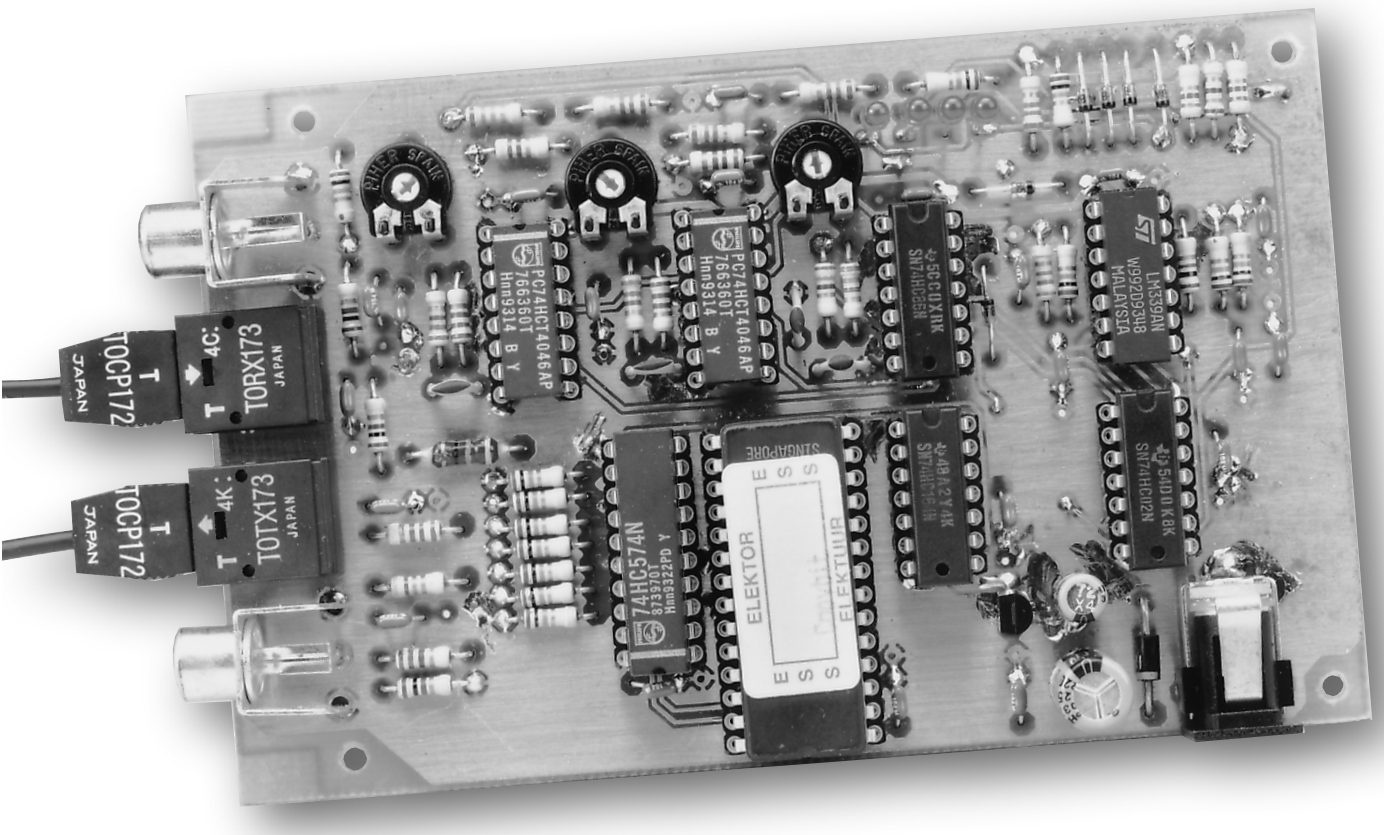


Figure 4. Illustration of the completed prototype board.

voltage at the relevant PLL (IC_3) is measured by comparators IC_{5b} and IC_{5d}. At the same time, the appropriate sampling frequency is indicated by D_2 or D_5.

The core of the copybit killer is the circuit for **decoding and disabling the copy-prohibit-bit**. This digital circuit consists of edge-triggered 8-bit shift register IC_7, 32 kbyte EPROM IC_8, and edge-triggered 8-bit latch IC_9.

Address lines A_0–A_7 of the EPROM are controlled via the shift register, while latch IC_9 provides the feedback of databits D_1–D_7 to addresses A_8–A_{14}. This arrangement, in conjunction with the software in the EPROM, ensures that the copy-prohibit-bit is recognized and disabled. The modified S/PDIF signal is available at pin 19 of the latch.

It would have been possible to use a programmed controller for this part ofthe copybit killer, but the cicuit as is forms a less expensive, readily available alternative to an EPLD. Moreover, programming an EPROM with conventional means is straightforward, which is an advantage that must not be underestimated.

The data for the EPROM is provided by a small Pascal program that produces a binary file of 32768 bytes. Constructors need not concern themselves with this since the programmed EPROM is readily available through our Readers' Services.

The **electrical-to-optical conversion** of the (modified) S/PDIF signal is effected by IC_{10}, an integrated transmitter from the same stable as the integrated input receiver.

The TTL output signal from latch IC_9 is converted by IC_{10} into an equivalent optical signal that can be passed on via a standard fibre-glass cable. Just as at the input, IC_{10} is shunted by a coaxial audio connector, K_2.

CONSTRUCTION

The copybit killer is best built on the printed-circuit board in **Figure 3**. Populating the board is straightforward by consulting the circuit diagram and parts list as well as the board itself.

All components are standard items. As mentioned earlier, IC_8 is available ready-programmed through our Readers' Services.

The functions of the four LEDs are:

D_2 sampling frequency is 48 kHz;
D_5 sampling frequency is 44.1 kHz;
D_9 sampling frequency is 32 kHz;
D_{10} input signal is absent or poor.

When the board has been completed, compare it with the photograph of the prototype in **Figure 4**.

The copybit killer may be powered by a mains adaptor via K_3. The adaptor output must not exceed 9–10 V to avoid the dissipation limit of IC_{11} being exceeded. Since the output of some adaptors is already 9 V when it is set to 6 V, it is advisable to actually measure the output.

The circuit draws a current of about 80 mA.

SETTING UP

Th trigger level at the input of the copybit killer is set with P_1. This is best done with the aid of an oscilloscope by making the pulses at the output (pin 8) of differentiating network IC_8 coincide with one another. This setting, which gives the least jitter., may be checked with other signal sources and sampling frequencies so as to obtain a good average.

Setting the VCO (IC_3) with P_2 is a precise operation. It has to be ensured that the voltage variation of about 220 mV at the output (pin 10) of IC_3 is symmetrical with respect to the input voltage to IC_{5b} and IC_{5d} (a window of about 80 mV) when the sampling frequency is switched from 44.1 kHz to 48 kHz and vice versa. This measurement is best carried out with a digital voltmeter.

The setting of the second VCO with P_3 is not so critical. Make sure, however, that the lighting of the relevant LED accords with the sampling frequency in use.

[970069]