digital potentiometer

Xicor's digitally controlled E^{2}POT ICs provide ergonomic and long-lasting alternatives to mechanical potentiometers. The ICs in the X9CMME series have a 7-bit counter with reversible count direction and a decoder that enables one of the 100 analogue switches.

The outputs of the analogue switches serve as the wiper of a potentiometer, while the inputs are linked to a potential divider composed of 99 equal resistors. The counter state may be stored in a non-volatile EEPROM, so that it can serve as the output value at a subsequent start.

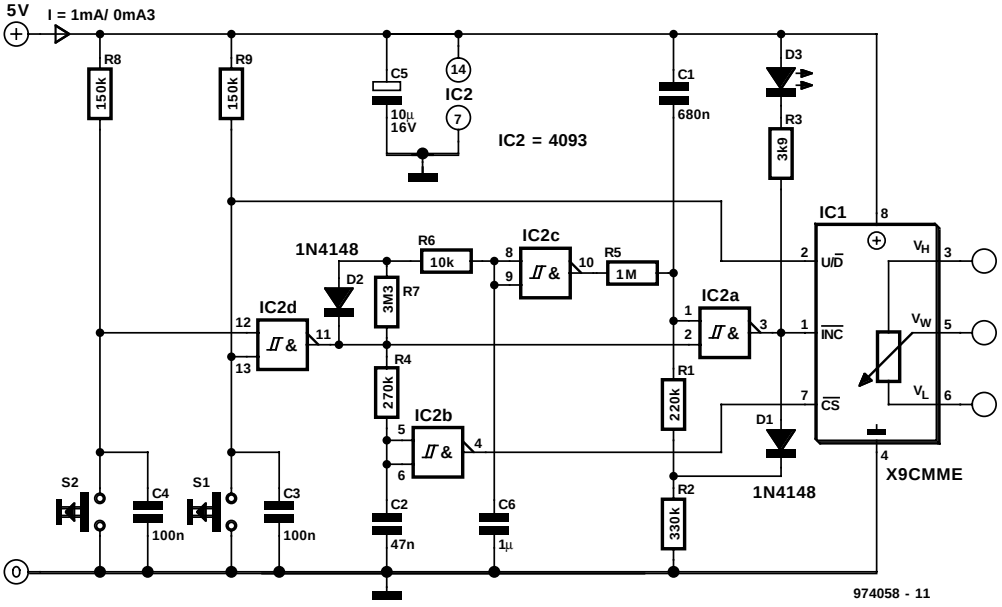
The X9CMM series is designed to operate from 5 V supply lines. The potential across the resistive divider must not exceed 10 V (only 4 V in case of the X9C102). The ON resistance of the analogue switch is about 40 Ω, so that the current through the wiper is limited to 1 mA.

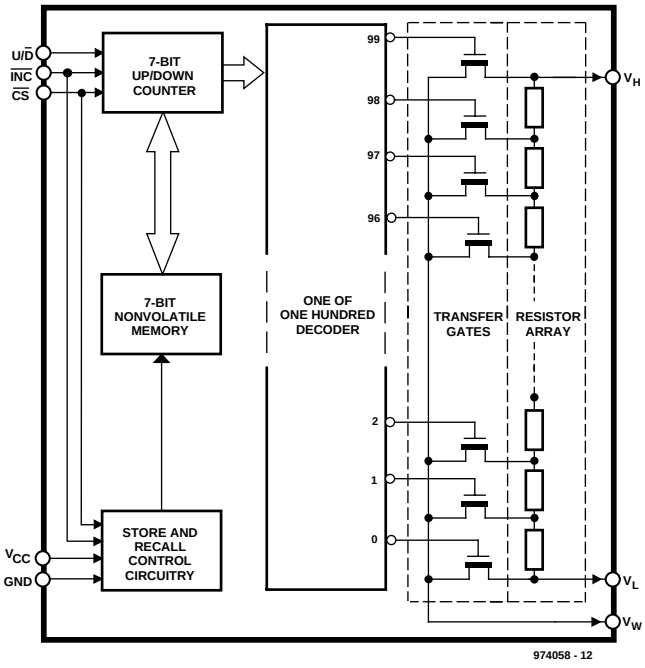
E^{2}POT ICs have three inputs for the digital drive. The level at U/D determines whether a trailing edge at clock input INC lowers or raises the counter state. This action only takes place if chip select input CS is low. A leading edge at CS arranges for the counter state to be stored when INC is high. When CS is high, the IC is in the standby mode.

The circuit diagram shows a complete digital potentiometer based on a Type X9CMME. It is provided with two controls, S_1 and S_2, an optical indicator and a delayed frequency change-over of the clock generator.

When keys S_1 and S_2 are open, resistors R_8 and R_9 hold the inputs of IC_{2d}, a NAND, as well as the U/D input of IC_1 high. The low level at the output of IC_{2d} disables clock generator IC_{2a}. Frequency determining capacitor C_1 is discharged in the quiescent state.

When one of the keys is pressed (S_1 firmly, S_2 gently), the output of IC_{2d} changes state, so that the clock generator and IC_1 (via IC_{2b}) are enabled. Capacitor C_1 is then charged via R_1 and R_2 until the input level of IC_{2a} goes low, whereupon the gate output linked to the clock input of IC_1 changes state (from low to high). When this happens, C_1 is discharged via R_1 and D_1 until the upper trigger level of IC_{2a} is attained. The gate then changes state again and the above action repeats itself.





The clock signal is optically monitored by D_3.

When the output of IC_{2c} is high, the gate draws a portion of the charging current from C_1, which results in the clock frequency at INC being relatively low.

At the same time that the generator is enabled, C_6 begins to be charged gradually via R_6 and R_7 until IC_{2c} changes states (from high to low). Circuit IC_2 then contributes to the charging current to C_1, whereupon the clock frequency increases: in the prototype, the frequency rose in four seconds from 1.3 Hz to 3.1 Hz.

When the keys are released, the clock generator stops. At the same time, C_6 is discharged rapidly via R_6 and D_2, so that the frequency is low again when the keys are operated anew.

The switch-off delay owing to R_4-C_2 enables the actual counter state to be stored by the internal logic.

The circuit draws a current of 0.3–1.0 mA. [Kühne – 974058]