S/PDIF-to-AES/EBU converter

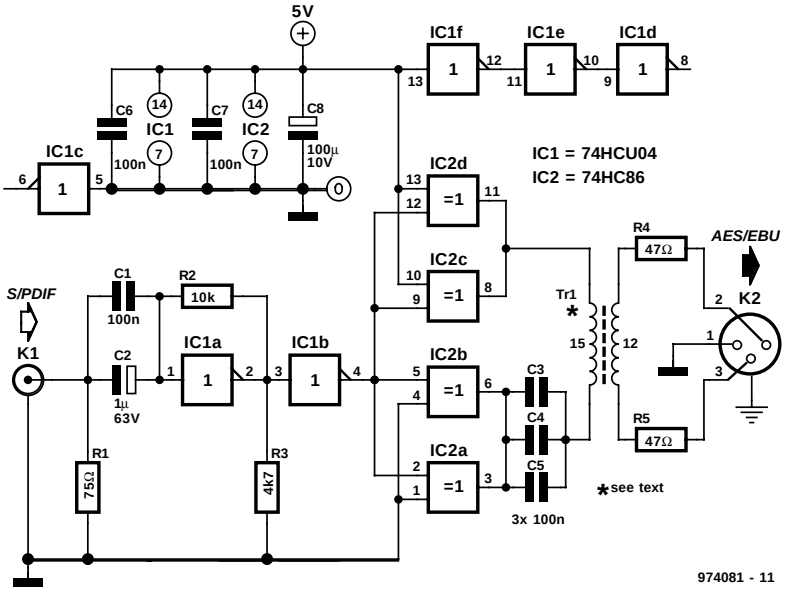
This magazine assumes that most readers use consumer appliances. However, in the case of the sample rate converter (October 1996), many readers have asked for a conversion from the asymmetrical S/PDIF format to the symmetrical (professional) AES/ EBU format and such a converter is presented here.

The timing and levels comply with the AES3-1992 Standard. This means that: (a) the output voltage must be 2–7 V_{pp} (transmitter load 100 Ω); (b) the rise and decay times must be 5–30 ns; (c) the output impedance must be 110 Ω ±20% (within the bandwidth of 0.1–6 MHz). These requirements are met in the design in the diagram (30 ns; 3.6 V_{pp}; 115 Ω respectively).

The circuit at the input, based on IC_1, converts the S/PDIF signal to HC levels. Op amp IC_{1a} is an analogue amplifier, while IC_{1b} raises the signal to the level of the supply lines. Resistor R_3 pulls IC_{1a} slightly from its centre of operation, so that the output buffer attains a logic level even in the absence of an input signal.

The buffer to drive the output transformer is formed by a symmetrical circuit based on IC_{2a}–IC_{2d}. This arrangement ensures that the rise and decay times are equal and that the output voltage is large enough. The use of XOR gates ensures that the transfer times for inverting and non-inverting of the output of IC_{1b} are equal. Since the primary transformer voltage is 9.5 V, the secondary voltage could be decreased slightly. This is beneficial for the linearity of the impedance and the bandwidth of the converter.

The transformer is wound on a Type G2-3/FT12 core: the primary on one side and the secondary on the other. Both windings consist of enamelled copper wire of 0.5 mm dia. The core can accommodate a tin-plate screen for maximum common-mode suppression. Regulations



require this to be ≥ –30 dB w.r.t. the nominal output level; in the present circuit it is –48 dB (with screen).

The output impedance, ignoring R_4 and R_5, is about 22 Ω. If a figure of exactly 110 Ω is wanted, R_4 and R_5 should have a value of 44.2 Ω.

Capacitors C_3–C_5 prevent any direct current flowing through the transformer in the absence of a signal as this would short-circuit IC_2. The use of three capacitors in parallel ensures that the impedance and loss resistance of them (ceramic, high-stability types) are low.

The AES/EBU signal is output via XLR connectors (to IEC268-12). Note that versions with male pins and female shells are used. Pin 1 is for the screen or the signal earth; pins 2 and 3 are for the signals – the phase is not important.

The circuit requires a 5 V power supply from which a current of about 26 mA is drawn.

If the converter is used with the sample rate converter published in the October 1996 issue or the 20-bit analogue-to-digital converter in the December 1996 issue, do not forget to use the CS8402A in the professional mode.

[Giesberts – 974081]